# RPC/SL71F16-xxx

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## 1 Introduction

## 1.1. General remarks

The content and presentation of this document has been carefully checked. No responsibility is accepted for any errors or omissions in the documentation.

Note that the documentation for the products is constantly revised and improved. The right to change this documentation at any time without notice is therefore reserved.

Syslogic is grateful for any help referring to errors or for suggestions for improvements. The following registered trademarks are used:

IBM-PC, PC/AT, PS/2	trademarks of IBM Corporation
I <sup>2</sup> C	trademark of Philips Corporation
CFast	trademark of CompactFlash Association CFA
PC/104	trademark of PC/104 Consortium
Intel Atom	trademark of Intel Corporation
Windows	trademark of Microsoft Corporation

All other trademarks appearing in this document are the property of their respective company.

## 1.2. Contents of this documentation

This document addresses to system integrators, programmers and instructed installation and maintenance personal working with the system. It provides information needed to configure, setup and program the RPC71 system.

### 1.3. Naming conventions

The exact product identifications are RPC/xxx or SDB/xxx. Throughout this documentation the product is reference through its marketing name "RPC71".

## 1.4. Documents and references

#### 1.4.1. Syslogic documentation

The following documents are *required* for correct installation and operation of the RPC71:

- CPU module documentation: DOC/ATOME6-E (cem\_atome6\_e.pdf)
- Wireless modul documentation: DOC/DOC\_IPC\_WLB-xxx (doc\_ipc\_wlbxxx\_USER\_MANUAL-1.0.pdf

#### 1.4.2. Datasheets

For additional and more detailed information on the Intel Atom processor and chipset the following documents are of interest:

- Datasheet Intel Atom Processor E6xx Series http://download.intel.com/embedded/processor/datasheet/324208.pdf#iid=3790
- Specification Update Intel Atom Processor E6xx Series <u>http://download.intel.com/embedded/processor/specupdate/324209.pdf?iid=387</u>



#### <u>6#iid=3876</u>

- Datasheet Intel Platform Controller Hub EG20T(PCH) <u>http://download.intel.com/embedded/chipsets/datasheet/324211.pdf#iid=3791</u>
- Specification Update Intel Platform Controller Hub EG20T (PCH) <u>http://download.intel.com/embedded/processor/specupdate/324209.pdf?iid=387</u> <u>6#iid=3876</u>
- Datasheet Intel 82574 GbE Controller Family <u>http://download.intel.com/design/network/datashts/82574.pdf</u>
- Datasheet NXP SJA1000 http://www.nxp.com/documents/data\_sheet/SJA1000.pdf
- Application Note AN97076: SJA1000 Stand-alone CAN controller http://www.nxp.com/documents/application\_note/AN97076.pdf

#### 1.5. Safety recommendations and warnings

The products are intended for measurement, control and communications applications in industrial environments. The products must be assembled and installed by specially trained people. The strict observation of the assembly and installation guidelines is mandatory.

The use of the products in systems in which life or health of persons is directly dependent (e.g. life support systems, patient monitoring systems, etc.) is not allowed.

The use of the products in potentially explosive atmospheres requires additional external protection circuitry which is not provided with the products.

In case of uncertainty or of believed errors in the documentation please immediately contact the manufacturer (address see chapter 11). Do not use or install the products if you are in doubt. In any case of misuse of the products, the user is solely liable for the consequences.

#### Important note

Ensure that the power supply is disconnected from the device before working on the device (connecting interfaces, replacing flash cards, opening the enclosure, etc.).

#### Important note

Please read the safety instructions of the power supply before installing/connecting the device.



#### Important note

Do not open the service cover unless you are instructed and entitled to do this. The service cover is intended for inserting the CFast Software storage card and the SIM card on initial operation of the product by an instructed person only.

#### **Important note**

Do not open the service cover unless you are instructed and entitled to do this. The service cover is intended for inserting the CFast Software storage card and the SIM card on initial operation of the product by an instructed person only.

#### 1.5.1. EMC

#### Important note

This is a Class A product and not intended to be used in domestic environments. The product may cause electromagnetic interference. Appropriate measures must be taken.

#### 1.5.2. Hot surface

#### Important note

Do not touch the surface of the device during operation. It may be hot and cause burns.



#### 1.5.3. Antennas

#### Important note

Do not operate the system without certified matching antennas connected to all antenna ports.

#### **1.6.** Electro-static discharge

Electronic boards are sensitive to Electro-Static Discharge (ESD). Please ensure that the product is handled with care and only in an ESD protected environment. Otherwise a proper operation is not guaranteed and the warranty is not applicable.



## 1.7. Life cycle information

#### 1.7.1. Transportation and storage

During transportation and storage the products must be in their original packing. The original packing contains a box with antistatic and shock-absorbing material. It is recommended, to keep the original packing in case of return of the product to the factory for repair. Note that the packing is recyclable.

#### 1.7.2. Operation

The operating environment must guarantee the environmental parameters (temperature, power supply, etc.) specified in the technical specification section of the product manuals.

The main functionality of the RPC system is defined by the application programs running on the processor board. The operating system and application programs are not part of the delivery by Syslogic but are defined, developed and tested by the customer or a system-integrator for each specific application. Refer to the respective documentation for more information.

#### 1.7.3. Maintenance and repair

The RPC system features error- and malfunction-detection circuitry. Diagnostic information gathered is transferred to the applications software where it can be used. In the rare case of a module hardware-failure or malfunction, the complete board should be exchanged. The faulty board must be returned to the factory for repair. Please use whenever possible the original packing for return of the product (ESD and mechanical protection).

#### 1.7.4. Warranty

Our products are covered by a world-wide manufacturer's warranty. The warranty period starts at the delivery time from our official distributor to the customer. The duration of the warranty period is specified in the respective product catalogs and the offers. All products carry a serial number for identification. The manufacturing data and deliveries are registered in a high level Quality Management System.

The warranty covers material and manufacturing defects. All products must be returned via the official distributor to the factory for repair or replacement. The warranty expires immediately if the products are damaged of operation outside of the specified recommended operating conditions. The warranty also expires if the date code or job number listed on the product is altered or rendered unintelligible. The warranty does not include damage due to errors in firmware or software delivered with the products.

#### 1.7.5. RoHS

The products of the RPC71 family are designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2002/95/EC).

#### 1.7.6. Disposal and WEEE

At the end of the life span the IPC products must be properly disposed. IPC products contain a multitude of elements and must be disposed like computer parts. Some of the IPC products contain batteries which should be properly disposed.



The products of the IPC/ML71 are not designed ready for operation for the end-user and intended for consumer applications. Therefore the Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable. But users should still dispose the product properly at the end of life.



## 2 **Product description**

### 2.1. RPC71 Systems

The RPC71 contains an enclosure, cabling and the motherboard. A list of main features of the motherboard can be found below:

## 2.2. Basic features of the RPC71

#### 2.2.1. CPU core

- Intel Atom E6xxT (Tunnel Creek) single core processor for mobile devices
- Industrial temperature range (-40..+85C)
- IA32 processor based on Intel's 45nm Hi-k metal gate silicon technology
- Multiple micro-ops per instruction are combined into one micro-op and executed in a single cycle
- in-order execution core
- high performance 32-bit 16-stage pipeline
- energy efficient branch prediction
- Up to 1.6GHz processor clock
- 32kB, 4-way instruction and 24kB, 6-way data L1 cache with parity
- 512kB, 8-way L2 cache with ECC
- 32-bit wide DDR SDRAM interface
- supports Intel Hyper Threading Technology (HTT), 2 threads
- supports Intel Virtualization Technology (VT-x)
- supports Enhanced Intel Speedstep Technology
- PCIe as front side bus, 2.5GB/s, 1.0a Base Specification compliant (4 x1 lanes)
- 32bit wide single channel DDR2 SDRAM interface

#### 2.2.2. Memory

- Up to 2 Gbyte DDR2 SDRAM on board (device width x16)
- 800MT/s data rate
- 32bit data width

#### 2.2.3. Graphics controller

- integrated Intel Graphics Media Accelerator 600 (Intel GMA600)
- power optimized 2D/3D graphics engine (max. 400MHz)
- integrated graphics device (IGD) includes LVDS and SDVO display ports
- LVDS max pixel clock 79.5MHz (equates to 1280x768 @ 85Hz)
- SDVO max. pixel clock 160MHz (equates to 1280x1024 @ 85Hz)
- Supports Streaming SIMD Extensions 2 and 3 (SSE2 and SSE3)
- Supports full hardware acceleration for H.264, MPEG2, MPEG4, VC1 and WMV9



- high performance 2D 64-bit graphics controller with backwards compatibility to VGA and SVGA standards
- Supports full hardware acceleration for H.264, MPEG2, MPEG4, VC1 and WMV9
- high performance 2D/3D 64-bit graphics engine

#### 2.2.4. CFast / SD Card / SATA

- 1 SATA port with CFast socket
- 1 SATA port with standard SATA connector
- 1 SD port with standard SD Card socket

#### 2.2.5. Integrated peripherals

- integrated peripheral controller (IPC) with PC/AT compatible DMA controllers (2 x 8237), interrupt controllers (2 x 8259) and timer/counter channels (8254)
- hardware watchdog configurable for 1.6s to 257s timeout, hardware reset activation
- temperature supervisor for software controlled power management

#### 2.2.6. Serial ports

 up to 4 serial RS232 ports (COM1 – COM4) with 16 byte receive and transmit FIFO (16550A compatible)

#### 2.2.7. Universal serial bus

- up to 4 USB V2.0 ports (OHCI/EHCI-Host Controller)

#### 2.2.8. Ethernet

- two 10/100 baseT Ethernet interfaces (Intel 82574)

#### 2.2.9. Firmware flash memory

- 8 MBit BootBlock Flash for BIOS and setup data

#### 2.2.10. Real time clock

- Year 2000 compliant Real Time Clock (PC/AT compatible)
- RTC backup supply through onboard GoldCap

#### 2.2.11. Configuration switches

- two rotary hex switches for customer application

#### 2.2.12. SPI

- SPI interface on internal header
- up to 8MB flash size allowed

#### 2.2.13. SMBus (I2C)

- SMBus v1.0 compliant (3.3V CMOS)
- SMBus interface on internal header



#### 2.2.14. LPC

- LPC 1.1 compliant interface
- LPC interface on internal header

#### 2.2.15. PC/104 Bus interface

- Subset of standard PC/104 bus interface
- DIN41612 bus connector

#### 2.2.16. CAN interface

- Two SJA1000 stand-alone CAN controller from NXP (Philips Semiconductor)
- BasicCAN or PeliCAN mode
- supports CAN 2.0A protocol in BasicCAN mode
- supports CAN 2.0B protocol in BasicCAN mode (29 bit identifier accepted)
- sully supports CAN 2.0B protocol in PeliCAN mode
- 16MHz clock frequency
- fixed I/O base addresses
- uses IRQ15
- ISO 11898-24V compatible interface
- optical isolation (1000VDC)
- configurable termination resistor, not terminated by default

#### 2.2.17. Digital I/O

- 4 digital 24V current sinking inputs
- 2 digital 24V current sourcing (high side) outputs
- galvanically isolated group of 4 inputs and 2 outputs

#### 2.2.18. Power supply

- Onboard isolated power supply with wide input range (10Vdc ... 30Vdc)
- Optional non-isolated power supply (9Vdc...30Vdc)
- Configurable power supply supervision Monitors either external power supply voltage or it can be used as external power fail or on/off input





Fig. 1 Block diagram (RPC71 basic features)

## 2.3. Addon features of the model RPC/SL71G16-xxx

#### 2.3.1. GPS

- **uBlox LEA-6N** GPS module

### 2.3.2. GPRS/UMTS

- uBlox LISA-U200 GPRS/UMTS module

### 2.3.3. WLAN

- Lesswire WiBear-11n WLAN module



## 2.4. Product variants

Device Function	RPC/SL71F16-A101E	SDB/SL71F16-WI1	Future products
Board	RPC/BL71-101E	SDB/BSL71-WI1	Future products
ETH1 10/100Mbit/s	Х	Х	
ETH2 10/100Mbit/s	Х		
RGMII	(X)		
COM1 (RS232)	Х	Х	
COM2 (RS232)	(X)	Х	
COM3 (RS232)	(X)		
COM4 (RS232)	(X)		
COM5 (isol. RS485)			
COM6 (isol. RS485)			
CAN1 (non isol.)		Х	
CAN1 (isol.)	Х		
CAN2 (non isol.)		Х	
CAN2 (isol.)	Х		
EG20T CAN	(X)		
USB1	Х	Х	
USB2	Х		
USB3	(X)		
USB4	(X)		
USB3 Hub			
PS/2			
DIO (2xOut, 4xIn)	(X)		
SPKR (Buzzer)			
VGA	Х	Х	
2-wire LVDS		Х	
Touch: CAN1		Х	
USB3			
COM5			
CFast	Х	Х	
SATA (std. Connector)	Х		
SATA		Х	
SD Card	Х		
LPC	(X)		
SPI	(X)		
SMB (I2C)	(X)		
ISA Bus	(X)		
Rotary Switch S1	Х		
Rotary Switch S2	Х		



Temp. sensor	Х	Х	
Watchdog	Х	Х	
PM Controller	Х	Х	
GoldCap	Х	Х	
10-30Vdc not isolated		Х	
10-30Vdc isolated	Х		
16-45Vdc isolated			
CPU	E680T/EG20T	E680T/EG20T	
	1.6GHz/1GB	1.6GHz/1GB	

#### Tab. 1 Feature List

(X) means that the interface is only available on an internal header. Please refer to the following chapter for a more detailed description of the interface and its connector.



## **3 Board description**

## 3.1. Overview

The RPC71 board hardware may be configured by software (BIOS) and by switch setting. Software configuration should always be done by using the BIOS Setup. The BIOS Setup can be entered by pressing  $\langle F2 \rangle$  at power-up.

The switches and connector locations are shown in the board layout drawing (Fig. 2).

#### **Important Note**

Always check the switch configuration of a freshly received board to comply with your system requirements before applying power, otherwise the system may get damaged or may fail to operate.

## 3.2. Board Dimensions

218mm x 120mm



## 3.3. Board Layout



Fig. 2 Top board layout (RPC71 base board)





Fig. 3 Bottom board layout (RPC71 base board)



## 3.4. List of connectors

Connector/Header ID	Туре	Comment
P1	2x2pin Micro-Fit 3.0, Rm3.00	Power Supply
	Molex 43046-0420	
P2	220pin SMX	CoreExpress
	Тусо 3-1827253-6	Bottom side
P3		SD Card
	FCI 10067847-011RLF	
P4	2x2pin PicoFlex, Rm1.27	EG20T CAN Interface
	Molex 90816-0304	
P5	2x2pin PicoFlex, Rm1.27	PS/2
	Molex 90816-0304	
P6	2x2pin Datamate, Rm2.00	ETH1 10/100 MBit/s
	Harwin M80-85 3 04 42 P	
P8	2x2pin Datamate, Rm2.00	ETH2 10/100 MBit/s
	Harwin M80-85 3 04 42 P	
P10	2x6pin Datamate, Rm2.00	VGA
	Harwin 80-82 8 12 45 P	
P11	2x4pin Datamate, Rm2.00	COM1
	Harwin M80-82 8 08 45 P	
P12	2x4pin Datamate, Rm2.00	COM2
	Harwin M80-82 8 08 45 P	
P13	2x4pin Datamate, Rm2.00	COM3
	Harwin M80-82 8 08 45 P	
P14	2x4pin Datamate, Rm2.00	COM3
	Harwin M80-82 8 08 45 P	
P15	2x4pin Micro-Fit 3.0, Rm3.00	FPDLinkII
	Molex 43045-0820	
P16	2x3pin Micro-Fit 3.0, Rm3.00	CAN1
	Molex 43046-0620	
P17	2x3pin Micro-Fit 3.0, Rm3.00	CAN2
	Molex 43046-0620	
P18	2x4pin Micro-Fit 3.0, Rm3.00	DIO Channel 1
	Molex 43046-0820	
P19	2x4pin Micro-Fit 3.0, Rm3.00	DIO Channel 2
	Molex 43046-0820	
P20	2x2pin Datamate, Rm2.00	USB Port 0
	Harwin M80-85 3 04 42 P	
P21	2x2pin Datamate, Rm2.00	USB Port 1
	Harwin M80-85 3 04 42 P	
P22	2x2pin Datamate, Rm2.00	USB Port 2
	Harwin M80-85 3 04 42 P	



Connector/Header ID	Туре	Comment
P23	2x2pin Datamate, Rm2.00	USB Port 3
	Harwin M80-85 3 04 42 P	
P24	SATA Plug, Rm1.27	SATA
	Molex 67800-5002	
P25	1x2pin Micro-Fit Header, Rm3.0	SATA
	Molex 43650-0226	
P26	2x6pin Dubox, Rm2.54	SATA
	FCI 89898-306ALF	
P27	CompactFlash Type I, 50pin	CFast
	3M N7G24-A0B2-RB-10-OHT	
P28	1x7 PicoBlade, R1.25	PIC Programming Header
	Molex 53398-0771	
P29	1x2pin Header, Rm2.54	Battery Header
	JST B 2B-XH-A	
P30	2x6pin PC/104 non stack through, press fit	ISA Bus
P31	2x6pin PC/104 non stack through, press fit	ISA Bus
	10-in Diseffer	
P32	18pin Piconex	RGMII
D22	Molex 90816-0318	
P33	/pin PicoBlade, Rm1.25 Moley 57709 0771	SPI, LVDS DDC
D24	Molex 55598-0771	
P34	6pin PicoBidde, Kill1.25 Moley 57709 0671	LED
D25	Drin DicoPlado Dm1 25	Duggor
P33	Zpili Picobidue, Killi.25 Molox 53308 0271	Buzzer
D26	Anin DicoPlado Pm1 25	SDI
P30	Molox 57308 0671	SFI
D27	Anin DicoPlado Dm1 25	SMD (I2C)
P3/	4piii Picoblade, Kiii.25 Moley 53308 0471	SIMB (I2C)
	2v72pip DC/104 pop stack through pross fit	IS A Duc
	2x32pin PC/104 non stack through proce fit	ISA Bus
	DINA1612 Style C Pm2 54	ISA Dus
TA/TD/TC/ YD	Eleo 21 9/50 129 071 025	ISA Dus
	LICU 21 0400 120 001 020	

Tab. 2 List of connectors

## 3.5. List of Headers

Switch ID	Туре	Comment
J1	1x2pin Header, Rm2.54	BIOS_INIT#
	Samtec, TSW-102-07-L-S	
J2	1x6pin Header, Rm2.54	JTAG
	Samtec, TSW-106-07-L-S	



Switch ID	Туре	Comment
J3	1x7pin Header, Rm2.54	LPC Bus
	Samtec, TSW-107-07-L-S	
J5	1x2pin Header, Rm2.54	BIOS_DISABLE#
	Samtec, TSW-102-07-L-S	

Tab. 3 List of header

## 3.6. List of LEDs

LED ID	Туре	Comment
DL1400	Green, SMD 0805	RUN#
	LTST-C170KGKT	
DL1401	Red, SMD 0805	STOP#
	LTST-C170KRKT	
DL500	Yellow, SMD 0805	Digital Output 0
	LTST-C170KSKT	
DL501	Yellow, SMD 0805	Digital Output 1
	LTST-C170KSKT	
DL504	Yellow, SMD 0805	Digital Input 0
	LTST-C170KSKT	
DL505	Yellow, SMD 0805	Digital Input 1
	LTST-C170KSKT	
DL506	Yellow, SMD 0805	Digital Input 2
	LTST-C170KSKT	
DL507	Yellow, SMD 0805	Digital Input 3
	LTST-C170KSKT	

Tab. 4 List of LEDs

## 3.7. List of Switches

Switch ID	Туре	Comment
S1	Hex Rotary Switch	User Switch
	Copal S-7050ETA	
S2	Hex Rotary Switch	User Switch
	Copal S-7050ETA	
<b>S</b> 3	Hex Rotary Switch	FPDLinkII
	Copal S-7050ETA	
S12	Hex Rotary Switch	External Power Input
	Copal S-7050ETA	
S14	Hex Rotary Switch	Power Management Controller
	Copal S-7050ETA	

Tab. 5 List of switches

## 4 Hardware description

## 4.1. Memory and I/O resources

#### 4.1.1. General memory layout and configuration

The RPC71 uses the same memory layout as a standard desktop PC. Onboard devices, DRAM, graphics controller and Boot Block Flash make use of the 4 GByte addressable memory space. Table 1 shows a typical configuration of the RPC71 with 2GB DRAM.

Add	ress	Size	Device / Register	Remarks
0000'0000h -	0009'FFFFh	640k	Main Memory (DRAM)	
000A'0000h -	000B'FFFFh	128k	VGA Video Memory	
000C'0000h -	000C'FFFFh	64k	Graphics BIOS	see paragraph 5.3
000D'0000h -	000D'FFFFh	64k	PCI Bus	
000E'0000h -	000F'FFFFh	128k	System BIOS	
0010'0000h -	7F4F'FFFFh	2036M	Main Memory (DRAM)	free Memory above 1M
7F50'0000	3FFF'FFFFh		8MB Graphic Memory (UMA)	do not access
			3MB System	
FFF0'0000 -	FFFF'FFFFh	1024k	<b>BIOS/BIOS Extensions</b>	do not access

Tab. 6Physical Memory Address Space Layout for RPC71

#### **Important note**

The main memory above 1M is not fully usable for applications. The main memory for applications is shared with the graphics memory (UMA: Unified Memory Architecture). The graphics memory can be either configured to 4MB or 8MB. The default value is 8MB. BIOS and other System devices use memory above 1MB. Depending on enabled or disabled functions in the BIOS the amount of additional memory used can vary.







#### 4.1.2. General I/O Layout and configuration

The RPC71's 64 kbyte I/O address space is mapped to the PC/104 bus address space as indicated in the table below. Note that 16 bit address decoding should be used on all PC/104 expansion boards to make efficient use of the I/O address space.



Addre	ess		Size	Device / Register	Remarks
0000h	-	000Fh	16 Bytes	Slave DMA (8237)	
0020h	-	0021h	2 Bytes	PIC master (8259)	command/status
0040h	-	0043h	4 Bytes	PIT (8254)	
0060h	-		1 Byte	Keyboard/mouse	data port
0061h	-		1 Byte	Port B	control
0064h			1 Byte	keyboard/mouse	command/status
0070h	-	0071h	2 Bytes	RTC RAM	address/data port
0072h	-	0073h	2 Bytes	high RTC RAM	address/data port
0080h			1 Byte	POST code	
0081h	-	0083h	2 Bytes	DMA low page	
0087h			1 Byte	DMA low page	
0092h			1 Byte	Port A	
00A0h	-	00A1	2 Bytes	PIC slave (8259)	Command/Status
00C0h			1 Byte	master DMA	
00C2h			1 Byte	master DMA	
00C4					
0200h	-	023F		free	
0278	-	027Fh	16 Bytes	reserved for LPT2	
02A8h	-	02AFh	8 Bytes	COM6	
02E0	-	02EFh	16 Bytes	free	
02F8	-	02FFh	8 Bytes	COM2	
0300h	-	036Fh		free	
0370h	-	0372h	3 Bytes	reserved for Floppy 2	
0374h	-	0375h	2 Bytes	reserved for Floppy 2	
0377h			1 Bytes	reserved for Floppy 2	
0378h	-	037Fh	8 Bytes	reserved for LPT2	
03A8h	-	03AFh	8 Bytes	COM5	
03B0h	-	03BBh	11 Bytes	VGA adapter	
03BCh	-	03BFh	4 Bytes	reserved for LPT3	
03C0h	-	03CFh	8 Bytes	VGA adapter	EGA
03D0h	-	03DFh	8 Bytes	VGA adapter	CGA
03E0h	-	03EFh	16 Bytes	free	
03F0h	-	03F2h	3 Bytes	reserved for Floppy 1	
03F4h	-	03F5h	2 Bytes	reserved for Floppy 1	
03F6h			1 Byte	primary IDE channel	
03F7h			1 Byte	reserved for Floppy 1	



03F8h	- 03F	Fh 8 Bytes	COM1	
0481h	- 048	3h 2 Bytes	DMA high page	
0487h		1 Bytes	DMA high page	
0489h	- 048]	3 Bytes	DMA high page	
048Fh		1 Byte	DMA high page	
04D0h	- 04D	1h 2 Bytes	PIC	Level/Edge
0500h	- 07F	Th 2048 Bytes	runtime registers SIO	Refer to Datasheet
0A78h		1 Byte	PnP	Configuration port
0CF8h	- 0CF	Fh 8 Bytes	PCI	Configuration register
2000h	- 2F	FF 4096 Bytes	PCI-PCI bridge	
3000h	- 3FF	Fh 4096 Bytes	PCI-PCI bridge	
4000h	- 401	Eh 29 Bytes	USB controller	
4020h	- 403	Eh 29 Bytes	USB controller	
4040h	- 405H	CH 29 Bytes	USB controller	
4060h	- 406	Eh 15 Bytes	IDE controller	
4070h	- 407	5h 7 Bytes	VGA controller	
7600h	- 76F	Fh 256 Bytes	Free	
7600h	- 76F	Fh 256 Bytes	CAN1	optional
7700h	- 77F	Fh 256 Bytes	Free	
7700h	- 77F	Th 256 Bytes	CAN2	optional
8200h	- 821	Th 16 Bytes	RPC/71 system register	
8220h	- 827	Th 128 Bytes	free	
0'D000h	- 0'EFFFh	1024 Bytes	Reserved for PCI device	VGA, LAN, USB, SATA

Tab. 7 I/O address space layout



## 4.2. Intel Atom E6xx Processor

The Intel Atom E6xx Processor Family (Codename Tunnel Creek) is a highly integrated x86 processor for embedded applications.



Fig. 5 Intel Atom Processor E6xx

## 4.3. Intel Platform Controller Hub EG20T

The Intel Platform Controller Hub EG20T companion device is designed to work with the Atom E6xx processor.



Fig. 6 Intel Platform Controller Hub EG20T



## 4.4. PCI/PCIe devices

All devices follow the PCI 2.2 and PCIe 1.0a specification. The BIOS (and/or OS) controls memory and I/O resources.



PCIe Lanes

#### Fig. 7 PCI Express System

PCI Device	Vendor ID	Device ID	Bus/	Interrupt	Comment
			Device/	INTline/	
			Function	INTpin	
Host Bridge	8086				
Graphic Controller	8086				
PCI/PCI Bridge	8086				
PCI/PCI Bridge	8086				
USB Controller	8086				
USB Controller	8086				
USB Controller	8086				
System Peripheral	8086				
System Peripheral	8086				
System Peripheral	8086				
PCI/LPC Bridge	8086				
SATA Controller	8086				
Ethernet Controller 1	8086	10D3			
Ethernet Controller 2	8086	10D3			

#### Tab. 8 PCI devices

The interrupt resources are assigned automatically by the BIOS and can be modified through a special setup screen (see chapter 4.5).



## 4.5. Hardware interrupts

The Intel Atom processor E6xx/EG20T chipset integrates two legacy 8259-compatible Programmable Interrupt Controllers (PIC). The registers of the PIC can be accessed through the I/O ports 020h and 021h resp. 0A0h and 0A1h.

Device	IRQ	PCI IRQ	Comment
8254 Timer	0	-	Legacy
Keyboard	1	-	Legacy
8259	2	-	Slave controller
UART	3	-	COM2
UART	4	-	COM1
UART	5	-	COM3
UART	6	-	COM4
PCI	7		PCI
RTC	8	-	Legacy
PCI_INT	9	-	PCI_INTB#
PCI	10	-	PCI_INTA# and PCI_INTC#
PCI	11	-	PCI_INTD#
Mouse	12	-	Legacy
FPU	13	-	Legacy
IDE	14	-	Primary IDE/SATA channel
CAN	15	-	CAN

#### Tab. 9 Hardware interrupt table

The interrupt and PnP resource are automatically allocated by the BIOS. In the setup screen "Andvanced  $\Rightarrow$  TunnelCreek Configuration  $\Rightarrow$  PCI Express Configuration" each interrupt can be reserved for a special peripheral device. During startup the PCI bus enumeration won't assign a reserved interrupt to a PnP/PCI device.

#### 4.6. DMA channels

DMA	Data Width	System Resource
0	8 bits	Available
1	8 bits	Available
2	8 bits	Available
3	8 bits	Available
4		Reserved, cascaded with channel
5	16 bits	Available
6	16 bits	Available
7	16 bits	Available

Tab. 10 DMA channels



## 4.7. Peripheral devices

#### 4.7.1. Scope

The peripheral devices described in this chapter are the core features of the RPC71 board. Meaning that they're available on all the derivates. Special features implemented only on one special board are described in a separate chapter of this documentation.

#### 4.7.2. VGA Interface

The analog VGA signals are supplied for direct connection of VGA compatible monitors. The BIOS provides the standard VGA API functions. All configuration is done by software (BIOS, VGA-BIOS).

#### 4.7.3. Device Connection

The VGA interface is available on a 12-pin female A-coded M12 connector (Molex Ultra-Lock).

Pin Number	Signal	Remarks
1	RED	VGA red
2	HSYNC	Horizontal sync
3	VSYNC	Vertical sync
4	GREEN	VGA green
5	DDC Clock	Clock
6	DDC Data	Data
7	BLUE	VGA blue
8	GND	
9	+5V	not fused
10	Analog GND R	
11	Analog GND G	
12	Analog GND B	

Tab. 11 VGA connector

#### Important Note

Maximum cable length allowed for VGA connection is 15 m. Use high quality VGA cables (with coaxial wires for RGB signals) for maximum EMI protection.



#### 4.7.4. Internal header P10

Pin Number	Signal	Remarks
1	RED	VGA red
2	HSYNC	Horizontal sync
3	VSYNC	Vertical sync
4	GREEN	VGA green
5	DDC Clock	Clock
6	DDC Data	Data
7	BLUE	VGA blue
8	GND	
9	+5V	not fused
10	Analog GND R	
11	Analog GND G	
12	Analog GND B	

Tab. 12 Internal VGA header



## 4.8. 2-Wire LVDS

The RPC71 supports a Low Voltage Differential Signaling (LVDS) interface with a pixel color depth of 18 and 24 bits. The maximum resolution is 1280x768 @ 60Hz. The pixel clock is specified between 19.75MHz up to 80MHz. The LVDS signals are serialized by the DS90UR907. 2-wire LVDS is also known as FPDLink II.

#### 4.8.1. Device Connection

The 2-wire LVDS interface is available on a 12-pin female A-coded M12 connector (Molex Ultra-Lock).

Pin Number	Signal	Remarks
1	+V24	24Vdc
2	+V24	24Vdc
3	GND	
4	GND	
5	TOUCHA	Positive Touch signal
6	TOUCHB	Negative Touch signal
7	FPDL_DOUTP	Positive LVDS signal
8	FPDL_DOUTN	Negative LVDS signal

Tab. 13 2-wire LVDS connector

#### 4.8.2. Options for Touch Signals

- CAN1
- USB3
- COM5

#### 4.8.3. Configuration Options for 2-wire LVDS

Only if S3 is assembled.

Switch S3	Configuration	Remarks
0	VOD=+/-300mV	
	LSB on RXIN3+/-	
	normal mode, control signal filter disabled (DS90UR908Q,	
	DS90UR906Q)	
1	VOD=+/-300mV	
	LSB on RXIN3+/-	
	normal mode, control signal filter enabled (DS90UR908Q,	
	DS90UR906Q)	
2	VOD=+/-300mV	
	LSB on RXIN3+/-	
	backwards compatible GEN2 (DS90UR124, DS99R124)	


3	VOD=+/-300mV	
	LSB on RXIN3+/-	
	backwards compatible GEN1 (DS90C124)	
4	VOD=+/-300mV	
	MSB on RXIN3+/-	
	normal mode, control signal filter disabled (DS90UR908Q,	
	DS90UR906Q)	
5	VOD=+/-300mV	
	MSB on RXIN3+/-	
	normal mode, control signal filter enabled (DS90UR908Q,	
	DS90UR906Q)	
6	VOD=+/-300mV	
	MSB on RXIN3+/-	
	backwards compatible GEN2 (DS90UR124, DS99R124)	
7	VOD=+/-300mV	
	MSB on RXIN3+/-	
	backwards compatible GEN1 (DS90C124)	
8	VOD=+/-450mV	
	LSB on RXIN3+/-	
	normal mode, control signal filter disabled (DS90UR908Q,	
	DS90UR906Q)	
9	VOD=+/-450mV	
	LSB on RXIN3+/-	
	normal mode, control signal filter enabled (DS90UR908Q,	
	DS90UR906Q)	
A	VOD=+/-450mV	
	LSB on KXIN3+/-	
D	backwards compatible GEN2 (DS90UR124, DS99R124)	
В	VOD=+/-450mV	
	LoB on KAIN5+/-	
C	backwards compatible GEN1 (DS90C124) VOD=1/450mV	
C	MSR on PVIN3 /	
	normal mode, control signal filter disabled (DS0011D0020	
	DS001R0060)	
D	$VOD = \pm / 450 \text{mV}$	
D	$MSB \text{ on } RXIN3\pm/-$	
	normal mode, control signal filter enabled (DS001)R0080	
	DS901IR9060)	
F	VOD - +/-450mV	
L	MSB  on  RXIN3+/-	
	backwards compatible GEN2 (DS0011P124 DS00P124)	
F	$VOD = \pm/-450 \text{mV}$	
1	MSB on RXIN3+/-	
	hackwards compatible GEN1 (DS90C124)	
	ouckwards comparior OLITT (D5/0C124)	



Tab. 14 2-wire LVDS configuration

## 4.8.4. Default Configuration

- $[CFG1, CFG0] = [1,0] \rightarrow backwards compatible GEN2 (DS90UR124, DS99R124)$
- RID = D4hex
- BISTEN =  $0 \rightarrow$  BIST mode disabled
- MAPSEL =  $0 \rightarrow$  LSB on RXIN3+/-
- VODSEL =  $0 \Rightarrow$  LVDS VOD = +/-300mV
- De-emph =  $0 \rightarrow$  De-Emphasis enabled
- Touch signals from CAN1 interface





# 4.9. CFast-interface

Two SATA ports are available. The support SATA 1.5Gps Generation 1 and 3Gbps Generation 2 speeds and are compliant with the Serial ATA Specification 2.6 and AHCI Revision 1.1. A CFast Flash card may be directly plugged in the on board CFast connector P27.

Tested CFast cards are:

- Cactus Technologies KC-series
- Western Digital SiliconDrive A100-7150 series (EOL)
- Apacer E

## 4.9.1. Device connection

Pin Number	Signal	Remarks
S1	SGND	Signal GND
S2	RxP	Receive +
<b>S</b> 3	RxN	Receive -
S4	SGND	Signal GND
<b>S</b> 5	TxN	Transmit -
<b>S</b> 6	TxP	Transmit +
<b>S</b> 7	SGND	Signal GND
PC1	CDI	Card Detect In
PC2	GND	
PC3	nc	
PC4	nc	
PC5	nc	
PC6	nc	
PC7	GND	Device GND
PC8	LED1	LED Output
PC9	LED2	LED Output
PC10	IO1	Reserved I/O (not connected)
PC11	IO2	Reserved I/O (not connected)
PC12	IO3	Reserved I/O (not connected)
PC13	PWR	Device Power
PC14	PWR	Device Power
PC15	PGND	Device GND
PC16	PGND	Device GND
PC17	CDO	Card Detect Out

Tab. 15 CFast Socket P27



# 4.10. SATA

Standard SATA Data Connector. Uses SATA channel 1.

## 4.10.1. Connector pinout for P24

Pin Number	Signal	Remarks
1	GND	
2	TX+	Transmit +
3	TX-	Transmit -
4	GND	
5	RX-	Receive -
6	RX+	Receive +
7	GND	
8	G1	GND
9	G2	GND

Tab. 16 SATA connector P24

# 4.10.2. Connector Pinout for P25

Pin Number	Signal	Remarks
1	+V5	5Vdc
2	GND	

Tab. 17 SATA power connector

# 4.11. SATA Expansion

A SATA/PATA converter board for the use of CompactFlashs or a SATA/CFast converter board can be connected onto P26. Contact the manufacturer for further information. The SATA expansion uses SATA Channel 1.

## 4.11.1. Connector pinout for P26

Pin Number	Signal	Remarks
1	GND	
2	GND	
3	RXN	Receive -
4	RXP	Receive +
5	GND	
6	GND	
7	TXN	Transmit -
8	TXP	Transmit +
9	GND	



10	GND	
11	+V5	5Vdc
12	+V5	5Vdc

Tab. 18 SATA Expansion

## 4.12. SD Card

## 4.12.1. Connector pinout for for P3

Pin Number	Signal	Remarks
1	DATA3	Data 3
2	CMD	
3	GND	
4	VDD	
5	CLK	Clock
6	GND	
7	DATA0	Data 0
8	DATA1	Data 1
9	DATA2	Data 2
WP#	WP#	Write Protection
CD#	CD#	Card Detection

Tab. 19 SD Card

# 4.13. Serial port 1

The serial port COM1 has a fixed base address of 3F8H. It uses hardware interrupt 4. The resources can be modified in the BIOS setup.

## 4.13.1. Device connection

The Serial Port1 COM1 is available on 8-pin male A-coded M12 connectors (Molex Ultra-Lock).

Pin Number	Signal	Remarks
1	DCD*	Data Carrier Detect
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR*	Data Terminal Ready
5	GND	
6	DSR*	Data Set Ready
7	RTS*	Request To Send
8	CTS*	Clear To Send

Tab. 20 Serial Port COM1



## 4.13.2. Internal header P11

COM1 is available on internal headers (type Harwin Datamate).

Pin Number	Signal	Remarks
1	DCD*	Data Carrier Detect
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR*	Data Terminal Ready
5	GND	
6	DSR*	Data Set Ready
7	RTS*	Request To Send
8	CTS*	Clear To Send

Tab. 21 Serial Port COM1

# 4.14. Serial port 2

The serial port COM1 has a fixed base address of 2F8H. It uses hardware interrupt 3. The resources can be modified in the BIOS setup.

## 4.14.1. Device connection

The Serial Port1 COM2 is available on 8-pin male A-coded M12 connectors (Molex Ultra-Lock).

Pin Number	Signal	Remarks
1	DCD*	Data Carrier Detect
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR*	Data Terminal Ready
5	GND	
6	DSR*	Data Set Ready
7	RTS*	Request To Send
8	CTS*	Clear To Send

Tab. 22 Serial Port COM2



## 4.14.2. Internal header P12

COM2 is available on internal headers (type Harwin Datamate).

Pin Number	Signal	Remarks
1	DCD*	Data Carrier Detect
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR*	Data Terminal Ready
5	GND	
6	DSR*	Data Set Ready
7	RTS*	Request To Send
8	CTS*	Clear To Send

Tab. 23 Serial Port COM1

# 4.15. Serial port 3

The serial port COM3 has a fixed base address of 3E8H. It uses hardware interrupt 5. The resources can be modified in the BIOS setup.

## 4.15.1. Device connection

The Serial Port1 COM3 is available on 8-pin male A-coded M12 connectors (Molex Ultra-Lock).

Pin Number	Signal	Remarks
1	DCD*	Data Carrier Detect
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR*	Data Terminal Ready
5	GND	
6	DSR*	Data Set Ready
7	RTS*	Request To Send
8	CTS*	Clear To Send

Tab. 24 Serial Port COM3



## 4.15.2. Internal header P13

COM3 is available on internal headers (type Harwin Datamate).

Pin Number	Signal	Remarks
1	DCD*	Data Carrier Detect
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR*	Data Terminal Ready
5	GND	
6	DSR*	Data Set Ready
7	RTS*	Request To Send
8	CTS*	Clear To Send

Tab. 25 Serial Port COM3

# 4.16. Serial port 4

The serial port COM4 has a fixed base address of 2E8H. It uses hardware interrupt 6. The resources can be modified in the BIOS setup.

## 4.16.1. Device connection

The Serial Port1 COM4 is available on 8-pin male A-coded M12 connectors (Molex Ultra-Lock).

Pin Number	Signal	Remarks
1	DCD*	Data Carrier Detect
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR*	Data Terminal Ready
5	GND	
6	DSR*	Data Set Ready
7	RTS*	Request To Send
8	CTS*	Clear To Send

Tab. 26 Serial Port COM4



## 4.16.2. Internal header P14

COM1 is available on internal headers (type Harwin Datamate).

Pin Number	Signal	Remarks
1	DCD*	Data Carrier Detect
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR*	Data Terminal Ready
5	GND	
6	DSR*	Data Set Ready
7	RTS*	Request To Send
8	CTS*	Clear To Send

Tab. 27 Serial Port COM4

# 4.17. Digital I/O ports

Two digital I/O ports are available on the front. See programming section for register adresses. No configuration options are available for the digital I/O ports.

The simplified input circuitry of one input channel is shown in Fig. 8, the simplified output circuitry of one output channel is shown in Fig. 9.

Note that the digital output circuit requires a separate external power supply.



Fig. 8 Equivalent Input Circuit



Fig. 9 Equivalent Output Circuit



## 4.17.1. Device connection

The Digital I/O Ports are available on 8-pin male A-coded M12 connectors (Molex Ultra-Lock).

Pin Number	Signal	Remarks
1	Input 0	
2	Input 1	
3	Input 2	
4	Input 3	
5	Output 0	
6	Output 1	
7	+Vproc	Process Voltage
8	GND	Process Ground

Tab. 28 Digital I/O Ports (M12)

## 4.17.2. Internal header P18

Pin Number	Signal	Remarks
1	+Vproc	Process Voltage
2	Input 0	
3	Output 0	
4	Input 1	
5	GND	Process Ground
6	Input 2	
7	Output 1	
8	Input 3	

Tab. 29 Digital I/O Ports (P18)

# 4.18. USB interface

The RPC71 features an OHCI/EHCI compatible USB Hostcontroller having assigned the base address and IRQ at boot time by the PCI-BIOS. Four channels are available.



## 4.18.1. Device connection

The USB channels 1/2 are available on 4-pin female A-coded M12 connectors (Molex Ultra-Lock).

Pin Number	Signal	Remarks
1	Vbus	Not short circuit protected
2	D-	
3	D+	
4	GND	

Tab. 30 USB channel 1 and 2

## 4.18.2. Internal headers P20, P21, P22, P23

All USB channels are available on internal headers (type Harwin Datamate).

Pin Number	Signal	Remarks
1	D+	Not short circuit protected
2	D-	
3	Vbus	
4	GND	

Tab. 31 USB channels 1, 2, 3 and 4

#### Important note

The USB power supplies on P20, P21, P22 and P23 are not protected against short circuit.

#### Important note

Maximum cable length allowed for keyboard and mouse connection is 3 m. Use shielded cables for maximum EMI protection.

# 4.1. USB Hub interface

Optionally a USB Hub with the PhyBoost feature can be assembled on the base board. Through software configuration the output voltage swing of USB port 4 can be adjusted for rugged environments. Please contact Syslogic for further details and MOQ.

# 4.2. CAN interface

There is no firmware for the CAN interface. All setup functions have to be programmed by the user or configured by a third-party device driver.



### **Important Note**

For detailed information and configuration options of the SJA1000 Stand Alone CAN Controller please refer to the appropriate documentation 1.4.2.

## 4.2.1. I/O base address configuration

The registers of the CAN controller can only be accessed in the I/O address space. The I/O base addresses cannot be configured. CAN1 is located at I/O 7600hex and CAN2 at I/O 7700hex. Both interfaces are not terminated through a  $120\Omega$  resistor. This must be done externally.

#### 4.2.2. Interrupt configuration

Both channels use interrupt IRQ15.

## 4.2.3. Device connection

The CAN interfaces are available on three separate 5-pin female A-coded M12 connectors (Molex Ultra-Lock).

Pin Number	Signal	Remarks
1	-	
2	-	
3	CAN Ground	
4	CANH	
5	CANL	

Tab. 32 CAN interfaces

## 4.2.4. Internal headers P16, P17

Both CAN interfaces are available on internal headers.

Pin Number	Signal	Remarks
1	SHIELD	
2	+V24	Not fused
3	CAN Ground	
4	CANH	CAN high
5	CANL	CAN low
6	Nc	

Tab. 33 CAN interface



# 4.3. EG20T CAN

The EG20T has an integrated CAN controller. The signals are available on an internal header. For the use as a fully compatible CAN interface according to the standard the physical layer has to be implemented on an expansion board.



## 4.3.1. Internal header P4

Pin Number	Signal	Remarks
1	GND	
2	TX	Transmit
3	RX	Receive
4	GND	

Tab. 34 EG20T CAN interface

# 4.4. Ethernet interfaces

The RPC71 features two PCIe 10/100Mbit-Ethernet controller having assigned the base address and IRQ at boot time by the BIOS.

No configuration options are available for the Ethernet device.

Use standard CAT5 100 $\Omega$  shielded or unshielded Twisted Pair cabling. Use shielded twisted pair cabling for maximum EMI protection.

## 4.4.1. Device connection

The Ethernet interface are available on 4-pin female D-coded M12 connectors (Molex Ultra-Lock).

Pin Number	Signal	Remarks
1	TX+	
2	RX+	
3	TX-	
4	RX-	

Tab. 35 Ethernet twisted pair interface connector

Both Ethernet channels are also available on internal headers.

## 4.4.2. Internal headers (10/100MBit/s)

Pin Number	Signal	Remarks
1	MDI_P0	MDI Positive 0
2	MDI_N1	MDI Negative 1
3	MDI_N0	MDI Negative 0
4	MDI_P1	MDI Positive 1

Tab. 36 Ethernet twisted pair interface connector

MDI Media Dependent Interface

# 4.5. RGMII

Reduced Gigabit Media Independent Interface is routed from the CPU directly to P32 (Molex Picoflex 18pin, 90816-0318).



## 4.5.1. Internal header P32

Pin Number	Signal	Remarks
1	RGMII_RD0	Receive Data Input 0
2	RGMII_TD0	Transmit Data Output 0
3	RGMII_RD1	Receive Data Input 1
4	RGMII_TD1	Transmit Data Output 1
5	RGMII_RD2	Receive Data Input 2
6	RGMII_TD2	Transmit Data Output 2
7	RGMII_RD3	Receive Data Input 3
8	RGMII_TD3	Transmit Data Output 3
9	RGMII_RXC	Receive Reference Clock
10	RGMII_TXC	Transmit Reference Clock
11	RGMII_RXCTL	Receive Control Signal
12	RGMII_TXCTL	Transmit Control Signal
13	RGMII_MDC	Management Data Clcok
14	RGMII_MDIO	Management Data I/O
15	RGMII_RST#	Reset
16	+V3.3S	3.3V supply
17	GND	Ground
18	+V3.3S	3.3V supply

Tab. 37 RGMII

RGMII Reduced Gigabit Media Independent Interface The power supplies aren't fused.

# 4.6. Watchdog

The watchdog timer is factory set for a 1.6s timeout. Other timeout values can be programmed up to about 257s (see programming section). Once timed out, it activates the RPC71 hardware reset when enabled.

# 4.7. System Management Bus (I2C)

The SMBus host controller integrated in the E6xx allows the processor to communicate with SMBus Slaves. The interface is compatible with most I2C devices. The interface complies with the System Management Bus (SMBus) Specification 1.0.

Device Name	7 Bit Address	Description
DA6011	0x69	ATOM E6xx power chip
BIOS EEPROM	0x57	EEPROM for saving BIOS settings
DB400	0x6E	PCIe clock repeater controller

Tab. 38 SMBus connected slaves



## 4.7.1. Internal header P37

Pin Number	Signal	Remarks
1	+V_SMB	Power supply $+3.3V^{1}$
2	SMB_CLK	Clock
3	SMB_DAT	Data
4	GND	Ground

Tab. 39 SMBus/I2C interface connector

<sup>1</sup> Optional +5V, contact manufacturer for further information. The power supply isn't protected.

# 4.8. Serial Peripheral Interface

An external SPI memory device is available to store persistent data.

## 4.8.1. Internal header P36

Pin Number	Signal	Remarks
1	+V_SPI	Power supply $+3.3V^{-1}$
2	SPI_MOSI	
3	SPI_MISO	
4	SPI_CS#	Chip Select
5	SPI_CLK	Clock
6	GND	Ground

Tab. 40 SPI

<sup>1</sup> Optional +5V, contact manufacturer for further information. The power supply is not protected.

## 4.9. Buzzer

A standard buzzer (2048Hz, 80dV, 60mA) is optionally available. The buzzer is assembled onto the PCB. With P35 a different buzzer can be connected to the base board and can be mounted at a different place.



## 4.9.1. Internal header P35

Pin Number	Signal	Remarks
1	+V5S	Power supply +5V
2	SPKR	Speaker signal

Tab. 41 Speaker/Buzzer

The power supply isn't protected.

# 4.10. LED

The STOP#, RUN# and SATA activity LEDs can be located at the front of the location with a special adapter board. The LED signals are available on an internal header.

## 4.10.1. Internal header P34

Pin Number	Signal	Remarks
1	+V5S	Power supply +5V
2	RUN#	
3	+V5S	Power supply +5V
4	STOP#	
5	+V5S	Power supply +5V
6	SATA	

Tab. 42 Speaker/Buzzer

The power supplies aren't protected.



# 4.11. ISA Bus

The PC/104 bus interface of the IPC/BL71 allows expansion with a wide range of I/O and communications boards. The bus interface is described in the IEEE 996 and 996.1 standards documentation. The bus connector pinout is shown below.For single board applications only the power pins should be connected. See paragraph 8.1 for electrical specification.

Pi	n	Signal Name	Pi	n	Signal Name	Pin		Signal Name	Pin		Signal Name
						A1	8	IOCHCK#	B1	8	GND
P30			P31			A2	8	SD7	B2	8	RESETDRV
1	8	GND	1	8	GND	A3	8	SD6	B3	8	+5V
2	8	SMB_DAT	2	8	+5V	A4	8	SD5	B4	8	IRQ9
3	8	SMB_CLK	3	8	SMB_ALRT#	A5	8	SD4	B5	8	-5V (not used)
4	8	Vbatt	4	8	STOP*	A6	8	SD3	B6	8	DRQ2
5	8	+V12	5	8	+V12	A7	8	SD2	B7	8	-12V (not used)
6	8	GND	6	8	GND	A8	8	SD1	B8	8	0WS#
D0	8	GND	C0	8	GND	A9	8	SD0	B9	8	+12V (not used)
D1	8	MEMCS16#	C1	8	SBHE#	A10	8	IOCHRDY	B10	8	(KEY)
D2	8	IOCS16#	C2	8	LA23	A11	8	AEN	B11	8	SMEMW#
D3	8	IRQ10	C3	8	LA22	A12	8	SA19	B12	8	SMEMR#
D4	8	IRQ11	C4	8	LA21	A13	8	SA18	B13	8	IOW#
D5	8	IRQ12	C5	8	LA20	A14	8	SA17	B14	8	IOR#
D6	8	IRQ15	C6	8	LA19	A15	8	SA16	B15	8	DACK3#
D7	8	IRQ14	C7	8	LA18	A16	8	SA15	B16	8	DRQ3
D8	8	DACK0#	C8	8	LA17	A17	8	SA14	B17	⊗	DACK1#
D9	8	DRQ0	C9	8	MEMR#	A18	8	SA13	B18	8	DRQ1
D10	8	DACK5#	C10	8	MEMW#	A19	8	SA12	B19	8	REFRESH#
D11	8	DRQ5	C11	8	SD8	A20	8	SA11	B20	8	SYSCLK
D12	8	DACK6#	C12	8	SD9	A21	8	SA10	B21	8	IRQ7
D13	8	DRQ6	C13	8	SD10	A22	8	SA9	B22	8	IRQ6
D14	8	DACK7#	C14	8	SD11	A23	8	SA8	B23	8	IRQ5
D15	8	DRQ7	C15	8	SD12	A24	8	SA7	B24	8	IRQ4
D16	8	+5V	C16	8	SD13	A25	8	SA6	B25	8	IRQ3
D17	8	MASTER#	C17	8	SD14	A26	8	SA5	B26	8	DACK2#
D18	8	GND	C18	8	SD15	A27	8	SA4	B27	8	TC
D19	8	GND	C19	8	(KEY)	A28	8	SA3	B28	8	BALE
						A29	8	SA2	B29	8	+5V
						A30	8	SA1	B30	8	OSC
						A31	8	SA0	B31	8	GND
						A32	8	GND	B32	8	GND

## 4.11.1. Connector pinout for PA/PB/PC/PD

Tab. 43 PC/104 bus connectors



# 4.11.2. Connector pinout for P30

Pin Number	Signal	Remarks
1	GND	
2	CLK	SMB
3	DAT	SMB
4	VBATT	Battery
5	n.c.	
6	GND	

Tab. 44 ISA Bus extension

## 4.11.3. Connector pinout for P31

Pin Number	Signal	Remarks
1	GND	
2	+V5	
3	ALERT#	SMB
4	STOP#	Red LED
5	n.c.	
6	GND	

Tab. 45 ISA Bus extension

# 4.12. LPC

For factory us only. These pins **must not** be connected by the user.

# 4.12.1. Internal header J3

Pin Number	Signal	Remarks
1	LAD0	Address/Data 0
2	LAD1	Address/Data 1
3	LAD2	Address/Data 2
4	LAD3	Address/Data 3
5	FRAME#	Frame
6	RST#	Reset
7	CLK	Clock

Tab. 46 LPC

# 4.13. DDC/SPI

For factory us only. These pins **must not** be connected by the user.



## 4.13.1. Internal header P33

Pin Number	Signal	Remarks
1	LDDC_CLK	DDC
2	LDDC_DAT	DDC
3	GND	SPI
4	MISO	SPI
5	MOSI	SPI
6	CS#	SPI
7	CLK	SPI

Tab. 47 DDC/SPI

# 4.14. Power supply

The processor and its peripherals are powered by a galvanically isolated, integrated power supply which generates all the necessary voltages.

# 4.14.1. Device connection

The power must be connected to a 5-pin male A-coded M12 connector (Molex Ultra-Lock).

Pin Number	Signal	Remarks
1	GND	
2	+24VDC	+10V+32Vdc
3	GND	optional, may be left open
4	+24VDC_AUX	not supported, leave open
5	Power Fail/Remote on/off	power fail input,
		may be left open in "Power Fail"
		mode if not used

Tab. 48 Power supply connector

For normal operation the external power supply has to be connected to the pins 2 (+24VDC) and 1 (GND) of the connector.

Pin 5 is used as an input for either a power fail or remote on/off signal.

## 4.14.2. Internal header P1

Pin Number	Signal	Remarks
1	GND	
2	+24VDC	+10V+30V
3	+24VDC_AUX	optional auxiliary power supply
4	Power Fail/Remote on/off	optional power fail input

Tab. 49 Power supply connector



## 4.14.3. Non-isolated power supply

Instead of the DC/DC converter a synchronous buck controller can be soldered onto the board. For further information please contact the manufacturer.

#### 4.14.4. Reverse voltage protection

Power Supply is protected against applying reverse voltage. Max. Protection voltage is the same as specified as max. voltage for the power supply.

#### 4.14.5. Power supervision

The power management control unit (PCU) contains a RISC microcontroller and is implemented on the base board.

The PCU can be operated in two modes: power fail mode or remote on/off mode. The following two chapters describe their functionality in detail.

Switch	Configuration	Remarks
S12	position '1' = remote on/off mode	check chapter 4.14.7
	position '2' = power fail mode (default)	
	positions '3' to 'F' = reserved (do not use)	

Tab. 50 Power supply configuration

## 4.14.6. Power Fail

In power fail mode the microcontroller monitors the external power fail signal. The state of power fail signal can be access through the status register, I/O 8200h. In order to initiate a power fail the pin has to be pulled low. Pulling it high or leaving it floating has no effect on the flag or operation

## **Application example**



### Fig. 10 Typical power fail application

The application has to poll the power fail flag and call different functions according to the state of the flag.





# Fig. 11 Typical power fail flow

Additionally the onboard power management contol unit (PCU) can switch off the power supplies after a power fail is detected. For that the PCU has to be configured according to the parameters found in table 51.

## 4.14.7. Remote On/Off

With the remote on/off function the system can be switched on and off through an external control signal. When active the internal software goes from the run state into the shutdown state. After a predefined timeout the PCU switches the main power supply off (even if the systems hangs while closing or terminating services). The timeout can be configured through S14. Please us the timing diagrams on the next pages for further understanding.

- Pull the remote On/Off signal to the supply voltage to start the system.
- Pull the remote On/Off signal to 0V or leave it floating to switch the system off.

Typical applications where Remote On/Off is used are mobile applications such as vehicles. To use the full functionality of the Remote On/Off feature it is required to use the pfmon software (sample code for Windows Embedded Standard OS or driver for Linux are available). The software analyzes the state of the remote On/Off signal and triggers a proper shut down. Additionally it is possible execute user commands before shutting down such as logging off from the network, etc.



## **Application example**



Fig. 12 Application example: Remote On/Off

# 4.14.8. PCU Configuration (power fail and on/off mode)

Configure the PF Signal using S12 according to table 50. Select a timing setting using S14 according to table 51.

Config switch S14 position	t <sub>debounce_on</sub> On debouncing (setup)	t <sub>debounce_off</sub> Off debouncing (hold)	t <sub>startup</sub> Hold time until switch off signal is routed to processor, if system is still booting	t <sub>hard_off</sub> Timeout until switch off signal is generated from processor (after that hard off)	
0 (default)	-	-	-	-	
1	2 s	60 s	5 s	1 min	
2	2 s	60 s	60 s	5 min	
3	2 s	60 s	30 min	2 h	
4	2 s	60 s	2 h	2 h	
5 – F	N/a	n/a	n/a	n/a	

Tab. 51 PCU timing configuration through S14

When switch S14 is in position 0 the PCU is in bypass mode (required for power fail mode).



## Delay time explanation

t <sub>debounce_on</sub>	Delay time during off mode time to prevent the system form start accidentally.
t <sub>startup</sub>	During this time the system will not turn off again the hardware to prevent the
	operating system to be turned off during start up.
t <sub>boot</sub>	Time while the operating system is starting. This time is independent of the
	PCU.
t <sub>debounce_off</sub>	During this time it is possible to restore the power and interrupt the PCU to turn
	off the hardware. Do not shut down the operating system during this period
	because the power is not turned off if the On/Off signal is restored.
t <sub>hard_off</sub>	Starts after $t_{debounce_off}$ has expired. After $t_{hard_off}$ the hardware will be turned off
	independently if the On/Off signal has been restored.
T <sub>shutdown</sub>	Time the operating system requires to shut down. Is independent of the PCU.

- Startup sequence 1. 23 4 5 6 2. 3. VIN Ignit 4. 5. internal RUNNING 6. OF BOOTING OS state
- Fig. 13 Start-up timing diagram



Fig. 14 Shutdown timing diagram

- Power is supplied to the system.
- On/Off signal is provided.
- If stable for more than 2 seconds the internal supplies are enabled.
- The system will start booting
- Operating system has finished starting up
- t<sub>statup</sub> time has expired. Now the System is ready to be turned off again.
- . The On/Off signal is released. If restored during t<sub>debounce\_off</sub> the system continues normally.
- .  $t_{debounce_off}$  has expired. The hardware is waiting for  $t_{hard_off}$  to turn off the internal supplies
- . Operating system is down.
- . Hardware is turned off

## **Important Notes**

The operating system must support the remote on/off function.



# 4.15. GoldCap Battery Backup

A GoldCap Capacitor is used to support the Battery.

- Capacity 1F typ.
- Backup time (RTC) 18.7h typ.

# 4.16. Configuration switches

There are two rotary Hex-Switches for customer use available. The values can be read from a register at I/O address 820Ch. The higher nibble contains the value of S2, the lower nibble the value of S1.

## 4.17. Factory programming header

The programmable logic devices on the RPC71 board are factory programmed using some pins of the internal header J2. These pins **must not** be connected by the user.

Pin Number	Signal	Remarks
1	ТСК	do not use
2	TDO	do not use
3	TMS	do not use
4	TDI	do not use
5	3.3V	do not use
4	GND	do not use

Tab. 52 Factory programming header J2

# 4.18. GPS

The GPS function is supported by use of a complete and certified GPS module manufactured by uBlox. The model LEA-6N-0-000 is connected to the GPS interface of the mating UMTS module. The GPS module is accessed over a special communications channel of the UMTS module by use of AT commands to virtual COM ports.

See <u>http://www.ublox.com/en/gps-modules/pvt-modules/lea-6-family.html</u> for detailed specification and programming information.

The GPS antenna input is available on a designated QMA(f) connector. The antenna must match the requirements according to the uBlox documentation. The design is done for use of active antennas (3V).

## 4.19. GPRS/UMTS

The GPS function is supported by use of a complete and certified GPS module manufactured by uBlox. The model LISA-U200-01S-00 is connected to an internal USB interface of the mainboard. The UMTS module is accessed by use of AT commands to virtual COM ports. See <a href="http://www.ublox.com/en/wireless-modules/umtshsdpa-modules/lisa-u2-series.html">http://www.ublox.com/en/wireless-modules/umtshsdpa-modules/lisa-u2-series.html</a> for detailed specification and programming information.



The UMTS antenna input is available on a designated QMA(f) connector. The antenna must match the requirements according to the uBlox documentation.

- UMTS/HSPA 800/850/900/1700/1900/2100 MHz<sup>1</sup>
- GSM GSM 850/900/1800/1900 MHz

# 4.20. WLAN

The WLAN function is supported by use of a complete and certified WLAN module manufactured by Lesswire. The model WiBear-11n is connected to an internal USB interface of the mainboard through a SDIO-to-USB bridge controller.

See <u>http://www.lesswire.com/en/products/embedded-wireless-modules/wlan/wibear-11n/overview/</u> for detailed specification and programming information.

The WLAN antenna input is available on a designated QMA(f) connector. The antenna must match the requirements according to the Lesswire documentation.

- IEEE 802.11a/b/g/n WLAN
- Bluetooth 3.0+High Speed (HS)
- Bluetooth 2.1+EDR

# 4.21. Hardware limitations

## 4.21.1. ISA bus limitations

- The interrupt lines are pulled up with 8k2 resistors to Vcc (EISA specification) instead of 2k2 (IEEE 996)
- NMI (IOCHCK#) is not supported on the PC/104 bus
- 16 bit cycles are not supported on the PC/104 bus
- memory cycles are not supported on the PC/104 bus
- Only a predefined amount of I/O addresses are available on the PC/104 bus, please refer to the appropriate chapter for details



# **5** Programming information

# 5.1. Overview

The programming of the RPC71 board is done with standard memory and I/O read and write operations. Most configuration options are handled by the BIOS.

# 5.2. Interrupt resources

Please refer to chapter 4.5 for the table showing the usage of the RPC71's interrupts.

# 5.3. Memory resources

The general memory layout is shown in paragraph 4.1.1. The configuration of the memory layout is done by programming processor internal configuration registers and board configuration registers (see paragraph 5.4). This is done completely by the BIOS on system startup and must not be changed during operation. For operating systems requiring memory configuration (e.g. Windows CE) the memory layout shown in paragraph 4.1.1 must be considered.

# 5.4. I/O resources

This paragraph describes only the RPC71 system register and support functions not directly related to a specific peripheral device. The general I/O layout is shown in paragraph 0. Peripheral devices are discussed in paragraphs 4.7 and 5.4.4.

# 5.4.1. Overview of general registers

Address	Device / Register	Remarks
8200h	Status Register	
8201h	Control Register	Reset state $= 05H$
8202h	Function ID Register	
8203h	Watchdog Configuration Register	Reset state $= 80H$
8204h	Option ID Register	
8205h	Setup Register	Reset state $= 00H$
8206h	Revision ID Register	
8207h	Reserved	
8208h	Reserved	
8209h	Reserved	
820Ah	Reserved	
820Bh	I2C Register	for Temp Sensor
820Ch	Switch Register	do not write
820Dh	Reserved	do not access
820E820Fh	Reserved	do not access
8210h	Digital Input Register	
8211h82FFh	Reserved	do not access

Tab. 53 RPC71 System Registers

## 5.4.2. Overview CAN specific registers

The following registers are only available if the RPC71 board has a CAN interface implemented.



Address	Device / Register	Remarks
82E0h	Status Register	Only if CAN is
		available
82E1h	Reserved	do not access
82E2h	Function ID Register	Only if CAN is
		available
82E3h	Reserved	do not access
82E4h	Option ID Register	Only if CAN is
		available
82E5h	Reserved	do not access
82E6h	Revision ID Register	Only if CAN is
		available
82E782FFh	Reserved	do not access

Tab. 54 RPC71 CAN Specific System Registers



## 5.4.3. Register layout

# Status Register 8200h D7 D6 D5 D4 D3 D2 D1 D0 Access

D/	D0	D5	D4	D3	D2	DI	D0	Access
OVERTMP	LOBAT	1	WDG#	1	1	ERRINT#	PF#	Read
reserved								Write
1111'1111 (0xFF)								Reset

Description:

OVERTMP	Temperature Sensor Status Flag				
	Read	Write			
	0 = programmed temp. limit reached				
	1 = temperature ok (below limit)				
LOBAT	Battery Status Flag				
	Read	Write			
	0 = Battery voltage low				
	1 = Battery voltage ok				
WDG#	Watchdog Status Flag				
	Read	Write			
	0 = Watchdog has timed out				
	1 = Watchdog running or disabled				
	Reset by issuing a hardware reset (see				
	register 8204h) or by writing				
	Watchdog Configuration Register				
	820511.				
ERRINT#	Error Interrupt Status from ISA Bus (IO	CHCK#)			
	Read	Write			
	0 = Error Interrupt pending				
	1 = No error interrupt pending				
PF#	Power Fail Status Flag				
	Read	Write			
	0 = Power fail pending				
	1 = No power fail pending				
Reserved	Reserved, always write 0				



# **Control Register 8201h**

D7	D6	D5	D4	D3	D2	D1	D0	Access
0	WDTRIG	WDNMI	STOP	1	1	0	1	Read
Reserved ERREN# reserved								Write
1000'1101 (8Dh)								Reset

Description:

WDTRIG	Watchdog Trigger									
	Read	Write								
	current value	Any state change triggers the watchdog.								
WDNMI	Watchdog NMI Configuration									
	Read Write									
	0 = Watchdog activates hardware									
	reset									
	1 = not supported									
STOP	Stop# Signal State									
	Read	Write								
	0 = Stop# inactive (high), red	0 = Stop# inactive (high)								
	LED									
	1 = Stop# active (low), red LED	1 = Stop# active (low)								
reserved	Reserved, always write 0									



## Function ID Register 8202h

D7	D6	D5	D4	D3	D2	D1	D0	Access
FID[7:0] Function ID								Read
reserved, always write 0								Write
same as Read value								

Description:

FID

Function ID

Read	Write		
51h = general NETIPC board	reserved		

reserved

Reserved, always write  $\boldsymbol{0}$ 

# Watchdog Configuration Register 8203h

D7	D6	D5	D4	D3	D2	D1	D0	Access
WDLOCK	0	0	0	WDTO	WDTOUT[3:0] Watchdog Timeout Selection			
WDLOCK	reserved	reserved	reserved	WDTO	Write			
1000'0000 (80h)								Reset

Description:

#### WDLOCK

Watchdog Lock Flag (prevents disabling running Watchdog)

Read	Write
0 = Inactive, not locked	0 = do not lock
1 = Active, locked	1 = lock WDEN

WDTOUT

## Watchdog Timeout Selection

Read	Write
0 = 1.6s	0 = 1.6s
1 = 5s	1 = 5s
2 = 9s	2 = 9s
3 = 17s	3 = 17s
4 = 33s	4 = 33s
5 = 65s	5 = 65s
6 = 129s	6 = 129s
7 = 257s	7 = 257s

reserved

Reserved, always write 0

Note: Any write operation to this register resets the Watchdog Status Flag in register 8200h.



# **Option ID Register 8204h**

D7	D6	D5	D4	D3	D2	D1	D0	Access
OID[7:0] Option ID								Read
reserved, always write 0								Write
same as Read value								Reset

Description:

OID

## Option ID

Read	Write
CCh = RPC71xx	A5h = Writing data A5h invokes a
	complete hardware reset (also clearing
	the Watchdog timeout status bit)

reserved

Reserved, always write 0



# Setup Register 8205h

D7	D6	D5	D4	D3	D2	D1	D0	Access
READY	WDEN	0	0	0	0	USBEN2/3	USBEN0/1	Read
READY	WDEN	0	0	0	0	USBEN2/3	USBEN0/1	Write
0000'0001 (00h)								Reset

Description:

READY Ready bit, green LED

Read	Write
0 = Inactive, green LED off	0 = Deactivate green LED
1 = Active, green LED on	1 = Activate

WDEN

Watchdog enable

Read	Write
0 = Watchdog disabled	0 = Disable watchdog
1 = Watchdog enabled (running)	1 = Enable watchdog

USB\_EN2/3 USB Ports Power Enable (all ports)

Read	Write
0 = USB  port  2/3  power off	0 = all USB ports power off
1 = USB port  2/3  power on	1 = all USB ports power on

#### USB\_EN0/1

USB Ports Power Enable (ports 0/1, read only)

Read	Write
0 = USB  port  0/1  power off	X = don't care, all USB ports are
1 = USB  port  0/1  power on	controlled by bit USB_EN2/3.
	This bit is reserved for a future version
	where the USB ports 0/1 may be
	controlled separately.

#### reserved

Reserved, always write 0



# **Revision ID Register 8206h**

D7	D6	D5	D4	D3	D2	D1	D0	Access
RID[7:0] Revision ID								Read
reserved, always write 0								Write
same as Read value								Reset

Description:

RID

## Logic Design Revision ID

Read	Write		
see Tab. 66	reserved		

reserved

Reserved, always write 0



# I2C Register 820Bh

D7	D6	D5	D4	D3	D2	D1	D0	Access
SCLO	SDAO	SCL	SDA	1	1	1	1	Read
SCLO	SDAO	Reserved, always write 1				Write		
xFh							Reset	
Description:								

SCLO	Clock Port Output State					
	Read	Write				
	0 = Pin state = low	0 = Output latch state $= $ low				
	1 = Pin state = high	1 = Output latch state = high				
		(open collector)				
SDAO	Data Port Output Port Latch State					
	Read	Write				
	0 = Pin state = low	0 = Output latch state $= $ low				
	1 = Pin state = high	1 = Output latch state = high				
		(open collector)				
SCL	Clock Port Pin State					
	Read	Write				
	0 = Pin state = low					
	1 = Pin state = high					
SDA	Data Port Pin State					
	Read	Write				
	0 = Pin state = low					
	1 = Pin state = high					
reserved	Reserved, always write 0					


#### Switch Register 820Ch

D7	D6	D5	D4	D3	D2	D1	D0	Access
S2_3	S2_2	S2_1	S2_0	S1_3	S1_2	S1_1	S1_0	Read
reserved, always write 0								Write
same as Read value								Reset

Description:

S2_3	Switch S2, bit 3						
	Read	Write					
	Data 2 <sup>3</sup>						
S2_2	Switch S2, bit 2						
	Read	Write					
	Data 2 <sup>2</sup>						
S2_1	Switch S2, bit 1						
	Read	Write					
	Data 2 <sup>1</sup>						
S2_0	Switch S2, bit 0						
	Read	Write					
	Data 2 <sup>0</sup>						
S1_3	Switch S1, bit 3						
	Read	Write					
	Data 2 <sup>3</sup>						
S1_2	Switch S1, bit 2						
	Read	Write					
	Data 2 <sup>2</sup>						
S1_1	Switch S1, bit 1						
	Read	Write					
	Data 2 <sup>1</sup>						
S1_0	Switch S1, bit 0						
	Read	Write					
	Data 2 <sup>o</sup>						

Reserved Reserved, always write 0

#### Digital Input Register 8210h

D7	D6	D5	D4	D3	D2	D1	D0	Access
DIN2[3:0]						Read		
reserved						Write		
same as Read value					same as F	Read value		Reset

Description:

DIN2	Digital Inputs Group DIO2					
	Read	Write				
	0 = input low or open					
	1 = input high					

DIN1

Digital Inputs Group DIO1

Read	Write
0 = input low or open	
1 = input high	

Reserved Reserved, always write 0

### 5.4.4. CAN register layout

#### **CAN Status Register 82E0h**

D7	D6	D5	D4	D3	D2	D1	D0	Access
1	1	1	CAN2_IRQ	1	1	1	CAN1_IRQ	Read
reserved, always write 0								Write
same as Read value							Reset	

Description:

CAN2\_IRQ CAN Channel 2 Interrupt Request

Read	Write
0 = IRQ pending	
1 = no IRQ pending	

CAN1\_IRQ

CAN Channel 1 Interrupt Request

R	ead	Write
0	= IRQ pending	
1	= no IRQ pending	

Reserved, always write 0

This register is only available on devices (and boards) where a CAN interface is implemented.



#### CAN Function ID Register 82E2h

		-						
D7	D6	D5	D4	D3	D2	D1	D0	Access
CFID[7:0] Function ID							Read	
reserved, always write 0							Write	
same as Read value								Reset

Description:

#### CFID CAN Function ID

Read	Write
6Ah = IPC/NETSBC-7AC	

Reserved, always write 0

This register is only available on devices (and boards) where a CAN interface is implemented.

CAN Option Register 82E4h								
D7	D6	D5	D4	D3	D2	D1	D0	Access
IO_MEM2*	0	0	1	IO_MEM1*	0	0	1	Read
reserved, always write 0							Write	
same as Read value								Reset

Description:

IO\_MEM2\* CAN Channel 2 Adressing Mode

Read	Write
$0 = I/O \mod$	
1 = not available	

#### IO\_MEM1\* CAN Channel 1 Adressing Mode

Read	Write
$0 = I/O \mod$	
1 = not available	

#### Reserved

Reserved, always write 0

This register is only available on devices (and boards) where a CAN interface is implemented.



CAN Revision ID Register 82E6h					
D7 D6 D5 D4 D3 D2 D1 D0 A	Access				
CRID[7:0] Function ID					
reserved, always write 0					
same as Read value					

Description:

RID

CAN Revision ID

Read	Write
see Tab. 66	

Reserved Reserved, always write 0

This register is only available on devices (and boards) where a CAN interface is implemented.

### 5.5. Peripheral devices

#### 5.5.1. Serial ports

The Serial Port interfaces use the standard PC/AT register set. The Serial Port controller is compatible with the standard 16C550A UART with 16 byte receive and transmit FIFOs. For detailed programming information please refer to the IBM PC/AT Technical Reference, the Texas Instruments TL16C550C datasheet or similar documentation. I/O base addresses and IRQ can be modified through BIOS.

#### 5.5.2. Ethernet interfaces

On the RPC71 board the Ethernet interfaces use the Intel 82574 Ethernet Controller. For detailed programming information and drivers check <u>www.intel.com</u>.



#### 5.5.3. Temperature sensor

The Temperature Sensor is built up using an LM75 compatible temperature sensor programmable through an I2C interface. The I2C interface programming is done through the I2C Register of the main board. The LM75 can be accessed at the I2C address 00h. For detailed programming information please refer to the National Semiconductor LM75 datasheet or similar documentation.

Poweron default setting for OVERTMP\* is 80°C chip temperature.

I2C Address	Device	Remarks
00h	LM75	

Tab. 55 I2C Address Space

#### 5.5.4. Watchdog

The watchdog is disabled by default on poweron and must be enabled either by the BIOS or by the application program.

The desired timeout may be configured by programming the watchdog configuration register. If watchdog programming is done from application software level, the watchdog configuration must be programmed before enabling the watchdog. The watchdog is enabled by setting the WDEN bit in the Setup Register.

The watchdog generates a hardware reset if it is not triggered within the configured timeout window. Triggering is done by toggling the WDTRIG bit in the Control Register. The application must check the WDG\* bit in the Status Register upon startup to identify the Watchdog as the source of the reset, and it must issue a hardware reset (by writing the value 0a5h to the Option ID Register) or write to the watchdog configuration register to clear the WDG\* flag. Otherwise the system resets again as soon as the watchdog is started.

The watchdog enable can be locked to prevent disabling by accident.

For sample code please contact Syslogic.



Fig. 15 Watchdog Blockdiagram

Programming flow sample:

- check watchdog status flag (read bit 4 of register 0x8200)
- if (watchdog status flag = active) log event and reset watchdog status flag



- set watchdog timeout and locking option (write value to register 0x8203)
- start watchdog (set bit 6 of register 0x8205)
- periodically trigger watchdog (toggle bit 6 of register 0x8201)
- if required (and not locked), stop watchdog (clear bit 6 of register 0x8205)

The watchdog can only initiate a hardware reset. The NMI option known from other Syslogic products is not supported.

Please contact the manufacturer for sample code.



# 6 Enclosure, assembly and mounting

### 6.1. **RPC71 dimensions**

The enclosure can house a complete industrial control system with many basic functions. The enclosure with its internal electronic system meets EMI/RFI electromagnetic standards according to the European "CE"- requirements (see paragraph 1.5).



Fig. 16 Dimensions RPC/SL71G16-xxx

#### **Important Notes**

Before assembling the whole enclosure with the electronic modules please read through the following paragraphs containing information about the assembling of the system.

### 6.1. High-strength screw retention

The screws used for enclosure assembly use high-strength screw retention (Precote). If the screws are removed they cannot be used again since the screw retention (Precote) is broken. New screws with Precote must be used.



# 7 Installation and cabling

### 7.1. Introduction

Installation and cabling of the RPC71 system has to be done with great care; the correct cabling is essential for high operational reliability and the correct grounding is necessary for protection. To meet the requirements of "CE"-certification all cables have to be shielded. The enclosure has to be connected to ground via the DIN-rail or mounting kit.

#### Important note

Before applying power to the RPC71 system, the mainboard must be configured correctly.

#### **Important notes**

To meet the requirements of RFI "CE"-certification, correct mounting, installation and cabling of the RPC71 system according to these guidelines is absolutely necessary.

### 7.2. Powering the RPC71 System

#### 7.2.1. General information

The "logic voltage", i.e. the power driving the electronic circuits (CPU and base board) is applied from a 24VDC power supply (e.g. 10VDC...30VDC). The internal power supply converts the input voltage to the logic voltage level. Remember that the power supply is isolated. For an unisolated version please contact the manufacturer.

#### 7.2.2. Power supply

The use of a power supply with the following requirements is mandatory:

- minimal power: 21W
- voltage range: 10...30Vdc
- efficiency > 88%
- integrated over-current limitation
- compliant with the directives 2004/1008/EC (EMC) and 2006/96/EC (LVD)
- compliant with the standards EN 61000-6-1, EN 61000-6-2, EN 61000-6-3 and EN 61000-6-4, FCC Part 15 Class B
- compliant with EN 60950-1



Syslogic recommends the use of the Syslogic DIN Rail power supply *PSU/DR24V60W* (input voltage: 230Vac, output voltage: 24Vdc, power: 60W).

Please make sure that the input voltage does not exceed the maximum specified voltage otherwise the base board could get damaged. If the input voltage drops below 10V the system doesn't work properly, correct operation cannot be guaranteed.

#### Important notes

Please read the safety and installation instructions of the power supply before connecting it to the IPC.

If connecting additional devices to the power supply the specified maximum power must not be exceeded.

#### 7.2.3. Power connection

For the exact pinout of the connector and header please go to chapter 4.14.



### 7.3. Cabling the interfaces

### 7.3.1. Connector locations



Fig. 17 Front view with connector markings (example)

51 C	1000406-1	31555752852	1222202 102464-47	
	GPS	UMTS	WLAN	
	$\oplus$	$\oplus$	$\oplus$	
	QMA-f	QMA-f	QMA-f	

Fig. 18 Rear view with connector markings (example)

Connector Marking	Interface Type	internal baseboard connector
USB1	USB channel 0	P20
USB2	USB channel 1	P21
ETH1	Ethernet 1	P6
ETH2	Ethernet 2	P8
X1	CAN1 (or COM5: RS485) <sup>1</sup>	P16
X2	CAN2 (or COM6: RS485) <sup>1</sup>	P17
VGA	VGA analog	P10
COM1	COM1: RS232	P11
PWR	Power Supply	P1
GPS <sup>2</sup>	GPS antenna	wireless board P200
GPRS <sup>2</sup>	GSM/GPRS/UMTS antenna	wireless board P230
WLAN <sup>2</sup>	WLAN antenna	P770

Tab. 56 Connectors (example)



<sup>1</sup> only if available, check product variants table. <sup>2</sup> only if available, check product variants table.

### 7.3.2. RPC/SL71F16-A101E

Connector Marking	Interface Type
PWR	Power supply
X2	CAN channel 2 (I/O base 0x7700)
X1	CAN channel 1 (I/O base 0x7600)
COM1	Serial port 1 (RS232)
DI/DO	Digital input/output
VGA	Display port
USB1	USB port
USB2	USB port
ETH1	Ethernet 1 (PCI device 13)
ETH2	Ethernet 2 (PCI device 12)

Tab. 57 RPC/SL71F16-A101E: Connectors

### 7.3.3. SDB/SL71F16-WI1

Connector Marking	Interface Type
PWR	Power supply
CAN2	CAN channel 2 (I/O base 0x7700)
CAN1	CAN channel 1 (I/O base 0x7600)
COM2	Serial port 2 (RS232)
COM1	Serial port 1 (RS232)
LVDS	2-Wire LVDS
VGA	Display port
USB2	USB port
USB1	USB port
ETH	Ethernet 1 (PCI device 13)

Tab. 58 SDB/SL71F16-WI1: Connectors



#### 7.4. Grounding

In some cases it is recommended to connect the shields of the cables to chassis potential at the entry point into the housing cabinet as shown in Fig. 19. If the cables enter a hermetically closed cabinet, use special 360 degree metal clamps (RFI protected types which contact to the cable shield).

#### **Important notes**

Grounding of the cables shields using "pig-tail wires" are not recommended because of their high impedance at high frequencies. It is better to clamp the shields onto a grounded copper rail.



Fig. 19 Additional grounding of the cable shields at the entry point of a cabinet.

### 7.5. Cabling of communication links

If the communication ports are unisolated ports, cable shields have to be connected to chassis potential on both sides of the interconnection cable. If the cable is very long, a thick copper wire (10 mm<sup>2</sup>) for potential adjustment is highly recommended. Fig. 20 shows an non isolated system with common chassis ground.

Some of the communication ports are galvanically isolated ports (for more information please refer to the documentation of the base board and the CPU board): in such cases the shield of



the interconnection cable must be wired to chassis potential only on one side of the cable. Fig. 21 shows an isolated system with independent grounds.

#### Important notes

Grounding of cable shields using "pig-tail wires" is not recommended because of their high impedance at high frequencies. It is recommended to clamp the shields onto a grounded copper-rail.



Fig. 20 Non isolated communication link with common chassis potential



Fig. 21 Isolated communication link



### 7.6. Cable length

The maximum cable length can be taken from the table below:

Device Marking	Interface Type	Cable Length	Shielded
VGA	VGA Display Interface	< 10m	Yes
LVDS	2-Wire LVDS	tbd	Yes
ETH1	Ethernet 1	> 30m (up to 100)	Yes
ETH2	Ethernet 2	> 30m (up to 100)	Yes
USB0	USB Interface	< 5m	Yes
USB1	USB Interface	< 5m	Yes
USB2	USB Interface	< 5m	Yes
USB3	USB Interface	< 5m	Yes
COM1	RS232	< 15m	Yes
COM2	RS232	< 15m	Yes
COM3	RS232	< 15m	Yes
COM4	RS232	< 15m	Yes
DI/DO	Digital I/Os	tbd	no
CAN1	CAN Interface	> 30m (up to 1000m @ 50kbit/s) <sup>1</sup>	Yes
CAN2	CAN Interface	> 30m (up to 1000m @ 50kbit/s) <sup>1</sup>	Yes
PWR	VDC/GND: Input Voltage	< 3m	No
	PF: Power Fail	< 3m	No
	VAUX: Auxilary Input	< 3m	No
	Voltage		

Tab. 59 Maximum cable length of all interfaces

<sup>1</sup> According to CAN in Automation (CiA).

### 7.7. Serviceable Parts

#### 7.7.1. General information

The RPC71 contains several serviceable or replaceable parts:

- CFast card (has to be ordered separately)
- SD card (has to be ordered separately)
- Fuse
- SIM card

#### Important notes

When opening the enclosure you're about to handle ESD sensitive devices. Be sure that appropriate precautions have been made to your working environment.

Ensure that the device is disconnected from the power supply.



#### Important notes

Precote screws are used with the RPC71 system. After opening the enclosure new screws must be used. Dispose the used screws appropriately.

#### 7.7.2. CFast/SD card

In order to exchange the CFast or SD card the following instructions must be executed.

- 1. Make sure that the device is not connected to a power supply!
- 2. Remove 12 Precote screws (M4x12, DIN912/ISO4762, BN612) on top of the enclosure.
- 3. Remove the top cover.
- 4. Exchange the CFast or SD card.



Fig. 22 Open side view with Reset button, battery and CFast

5. Close the top cover with the correct screws.



Handle the flash memory module with care. In order to simplify the removal of the memory module a small commercially available tape can be applied to the compact flash which allows an easy grab of the module.

#### 7.7.3. Fuse F1701

The onboard fuse prevents the destruction of the product in cause of a malfunction. The fuse must be replaced by an instructed person/technician and in an ESD protected environment. The fuse F1701 is located on the PCB as shown in the figure below.

- 1. Make sure that the device is not connected to a power supply!
- 2. Remove 12 Precote screws (M4x12, DIN912/ISO4762, BN612) on top of the enclosure.
- 3. Remove the top cover.
- 4. Carefully remove the fuse with a pair of tweezers or needle-nosed pliers.



Fig. 23 Open side view with Reset button, battery and CFast

5. Close the top cover with the correct screws.

Type for F1701: Littlefuse Nano<sup>2</sup> Slo-Blo 3A: 0452.003MRL

Please note that in the code above the package code for tape and reel and quantity 1000pcs is included.



For further information on how to replace the fuse please contact the manufacturer.

#### 7.7.4. SIM Card Installation (Optional)

For SIM Card installation a service cover can be done on special customer request.

It is highly recommended to shut down the system and remove power before removing the service cover.

On the figure the SIM card holder is marked in blue.

After having pushed the locking slider downside, the SIM card must be pushed in completely and secured by pulling the locking slider back up.

To remove the SIM card, the locking slider has to be pushed down. Then a short push on the SIM card will activate an ejection mechanism, making the card accessible for pulling it out of the card holder.



Access Panel for SIM Card Installation (Can be done on special customer request!)

#### Fig. 24 SIM card installation

Please mount the optional service cover before reapplying power and restarting the system.



# 8 Technical data

### 8.1. Electrical data

#### **Important Note**

Do not operate the RPC71 outside of the recommended operating conditions. Otherwise lifetime and performance will degrade. Operating the board outside of the absolute maximum ratings may damage the hardware.

#### Absolute maximum ratings (over free-air temperature range)

Parameter	symbol	min	nom	max	unit
general parameters					
power supply voltage	Vp	-0.5		30	V
DIO supply voltage (external supplied, isolated)	Vdio	-0.5		31	V
isolations					
power supply to chassis (AC, 60s, 500m a.s.l.,		500			Vrms
Ta=25°C)					
power supply to logic (AC, 60s, 500m a.s.l.,		500			Vrms
Ta=25°C)					
Ethernet to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
Ethernet to logic (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
CAN to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
CAN to logic (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
DIO to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
DIO to logic (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
temperature range					
storage temperature range	Tst	-40		85	°C

Tab. 60 General absolute maximum ratings



### **Recommended operating conditions**

Parameter	symbol	min	nom	max	unit
general parameters					
power supply voltage (isolated)	Vp	10	24	30 1	V
power supply voltage (non-isolated)	Vp	9	24	30 1	V
power supply interruption class (EN50155)			S1		
digital outputs					
DIO supply voltage (external supplied, isolated)	V(dio)	19	24	30	V
output current at DIO output (each output)	Io(dio)	0	250	300	mA
digital inputs					
high-level input voltage (=input ON)	Vih	15	24	30	V
low-level input voltage (=input OFF)	Vil	-10		10	V
temperature range					
operating free air temperature (Component Level)	Та	-40		85	°C
operating free air temperature (Ambient)	Та	-40		70	°C
operating temperature class (EN50155)			TX		

Tab. 61 General recommended operating conditions

<sup>1</sup> 1.25 \* Vp<sub>nominal</sub> acc. EN50155

The temperature range is dependent on the amount of power loss (heat) generated inside the enclosure.



### Electrical characteristics (over recommended operating range, unless otherwise noted)

Parameter	symbol	min	typ	max	unit
general parameters					
power dissipation	Р			17.5	W
power supply current (25VDC)	Ip			0.7	А
power supply current (36VDC)	Ip		0.4		А
under-voltage lockout	Vuvlo		17		V
power fail		2.3	Vext	Vext	V
- inactive state	$\mathrm{PF}_{\mathrm{high}}$	-0.5	0	2.7	V
- active state	$\mathrm{PF}_{\mathrm{low}}$				
remote on/off					
- on	ENon	8.5	Vext	Vext	V
- off	EN <sub>off</sub>	-0.5	0	7.1	V
backup current	I <sub>back</sub>		22	36	μA
LOWBAT* trip voltage		2.35	2.5	2.65	V
RTC trip point (RTC valid RAM and time flag)			2		V

Tab. 62 General electrical characteristics



# Switching characteristics (over recommended operating range, unless otherwise noted)

Parameter	Symbol	min	nom	max	
processor characteristics					
Processor clock	f <sub>cpu</sub>			1.6	GHz
memory clock (DDR800)	f <sub>mem</sub>			400	MHz
memory transfer rate				800	MT/s
PCIe clock (1 x lane)	fpcie			2.5	GBit/s
LPC bus clock	$f_{lpc}$			33	MHz
ISA bus clock	f <sub>isa</sub>			8.25	MHz
communication interface characteristics					
COM1/COM2 baud rate				115.2	kbaud
COM3/COM4 baud rate				115.2	Kbaud
LAN1/LAN2 baud rate		10		100	Mbit/s
CAN1/CAN2 baudrate, dependant on connected				1	Mbit/s
nodes and bus length					
CAN clock	f <sub>can</sub>			16	MHz
ISO high speed CAN signal		Refer	to ISO 1189	98-24V	
timer/clock characteristics					
Watchdog timeout (configurable)	Tw	1		257	S
Timer base clock 1	f <sub>clk1</sub>		14.318		MHz
Timer base clock 1 accuracy				+/-100	ppm
Timer base clock 2	f <sub>clk2</sub>		32.768		kHz
Timer base clock 2 accuracy				+/-20	ppm
Timer base clock 2 aging				+/-3	ppm/year
Real Time Clock base clock	f <sub>clk</sub>		32.768		kHz
Real Time Clock accuracy (25°C)				+/-20	ppm
Real Time Clock temperature coefficient				-0.04	$ppm/(^{\circ}C)^2$
Real Time Clock aging				+/-3	ppm/year
digital I/O characteristics					
input frequency (Vin=nom., duty ratio 1:1)	fimax	2			kHz
input pulse width (Vin=nom.)	tw	250			us
input pulse suppression (Vin=nom., duty ratio 1:20)		10			us
input on delay (Vin=nom.)	ton		100		us
input off delay (Vin=nom.)	toff		180		us
switching frequency (Us=24V, resistive load	fomax				kHz
250mA)		1			
switch on delay (Us=24V, resistive load 250mA)	ton			300	us
switch off delay (Us=24V, resistive load 250mA)	toff			400	us

Tab. 63 General switching characteristics



### Wireless operating conditions and characteristics (over recommended operating range, unless otherwise noted)

Please check module manufacturer documentation for detailed operating conditions and characteristics (<u>www.ublox.com</u>, <u>www.lesswire.com</u>).

### 8.2. EMI / EMC specification

#### 8.2.1. Relevant standards

The RPC71 has been designed to comply with the following standards:

-	EN 50121-3-2	Railway applications- Electromagnetic compatibility -
		Rolling stock – Apparatus
-	EN 13309:2010-12	Construction machinery- Electromagnetic compatibility of machines with internal electrical power supply
-	EN 61000-6-2	Electromagnetic compatibility (EMC), Part 6-2: Generic standards- Immunity for industrial environments
-	EN 61000-6-4	Electromagnetic compatibility (EMC), Part 6-4: Generic standards – Emission standard for industrial environments
-	CISPR 25:2008-03	Vehicles, boats and internal combustion engines – Radio disturbance characteristics

#### 8.2.2. Emission

Test	Limit	Performance	Remarks
		Criteria	
Stationary interference voltage on the AC	EN 50121-3-2		basic standard EN 55011
voltage terminals			
V-Network 0.15 – 30 MHz			
Power supply line			
Control and signal lines			
Radiated E-Field, horizontal and vertical	EN 50121-3-2		basic standard EN 55011
polarized			
E-Field-Antenna 30 – 1000 MHz			
EUT with all cables			

Tab. 64 Electromagnetic emission



### 8.2.3. Immunity

Test	Standard	Perfromance	Remarks
	Test level	Criteria	
Electrostatic discharge (ESD)	EN 61000-4-2		Compliant with
- indirect on coupling plane with contact	6kV Cont.	В	EN 50121-3-2
discharge			
- direct on case with air and contact	8kV Air (metal	В	
discharge	case)		
EUT with all cables			
Radiated electromagnetic field	EN 61000-4-3		Compliant with
80 - 1000 MHz, 80% AM (1kHz)	20V/m	А	EN 50121-3-2
EUT with all cables			
Radiated electromagnetic field	EN 50121-3-2		
1.4 - 2.1 GHz, 80% AM (1kHz)	10V/m	А	
2.1 - 2.5 GHz, 80% AM (1kHz)	5V/m	А	
EUT with connection cable			
Fast transients (EFT)	EN 61000-4-4		Compliant with
Common Mode, 5/50ns, repetition freq. 5kHz			EN 50121-3-2
Control and signal lines	2kV	А	
Power supply	2kV	А	
Surges	EN 61000-4-5		Compliant with
Pulse form 1.2/50us	2.0kV (ground)		EN 50121-3-2
Power supply	1.0kV	В	
All other signal lines (L>30m)			
Conducted radio frequency	EN 61000-4-6		Compliant with
150kHz - 80MHz, 1kHz 80% AM			EN 50121-3-2
Control and signal lines (L > 3m)	10V	А	
Power supply	10V	А	

Tab. 65 Electromagnetic immunity



### 8.3. Environmental specification

The RPC71 has been designed to meet with the following standards:

- EN 61373	Railway application – Rolling stock equipment: Shock and vibration tests
-EN 60068-2-1	Environmental testing – Part 2-1: Tests - Test A: Cold
-EN 60068-2-2	Environmental testing - Part 2-2: Tests - Test B: Dry heat
- EN 60068-2-14	Environmental testing – Part 2-14: Tests - Test N: Change of temperature
-EN 60068-2-17	Basic environmental testing procedures – Part 2-17: Tests – Test Q: Sealing
- EN 60068-2-27	Basic environmental testing procedures – Part 2-27: Tests - Test Ea and guidance: Shock and guidance
- EN 60068-2-30	Environmental testing – Part 2-30: Tests - Test Db: Damp heat, cyclic (12 + 12 hour cycle)
- EN 60068-2-64	Environmental testing – Part 2-64: Tests - Test Fh: Vibration, broadband random and guidance
- DIN 40050-9	Road vehicles; degrees of protection (IP-code); protection against foreign objects, water and contact; electrical equipment

### 8.4. Mechanical data

The enclosure can house a complete industrial control system with many basic functions. The enclosure with its internal electronic system meets EMI/RFI electromagnetic standards according to the European "CE"- requirements (see chapter 8.2). If you need detailed information of the enclosure do not hesitate to contact the manufacturer. We can provide you with the technical drawings.

#### 8.5. Protective Vent

The enclosure is protected by a protective vent (Gore PMF100444) which is designed to protect in the harshest environments while quickly and effectively equalizing the pressure in sealed enclosures.

Technical Data:

- Water proof and dust proof to IP69K
- Explosion proof Ex I M2 II 1D 2G EEx e I/II IP66
  - Ex-Approval (According to Council Directive 94/9/EC ATEX (95)





 $\langle \widehat{\epsilon_x} \rangle$  I M2 EEx eI  $\langle \widehat{\epsilon_x} \rangle$  II 2G EEx eII  $\langle \widehat{\epsilon_x} \rangle$  II 1D

- Water and oil repellant, Membrane type: ePTFE.
- Salt Spray Test (DIN 50-0-21). The microporous structure of the ePTFE membrane even keeps salt crystals from passing. Minimizing electrical malfunctions caused by salt corrosion.
- Typical airflow (dp = 70 mbar): 1700 ml/min
- Explosion approval (Directive 94/9/EC ATEX [95])
- Membrane characteristic: Oleophobic
- O-Ring material: Silicone 60 Shore A
- Temperature range: -40°C to 125°C
- RoHS

### 8.6. IP Protection Grade

RPC71 offers IP67 protection grade, the digit meaning is in detail:

- 6: Dust tight, No ingress of dust; complete protection against contact
- 7: Immersion up to 1 m. Ingress of water in harmful quantity shall not be possible when the enclosure is immersed in water under defined conditions of pressure and time (up to 1 m of submersion).

### 8.7. Chemical Resistance

RPC71 was tested to offer chemical resistance against the following substances:

- Battery Acid
- Cold cleaner solvent
- Coolant
- Brake Fluid
- Bio Diesel
- Diesel
- Gasoline
- Gear Lubricant oil
- Hydraulic fluid

For further information please contact the manufacturer.

### 8.1. PCB Coating

RPC71 PCBs may be coated with Electrolube DCA SCC3 Conformal Coating.

- High specification flexible modified silicone resin
- conformal coating
- UL746 approved
- May be ambient cured or heat cured for enhanced performance



- Excellent chemical and solvent resistance when heat cured
- May be soldered through of rework
- Extremely wide operating temperature range

For further information please contact the manufacturer.



## 9 Firmware

### 9.1. BIOS

#### 9.1.1. General information

The BIOS provided by Syslogic is based on the SecureCore Tiano from Phoenix Technologies. It has been customized to support onboard peripherals.

#### **Important note**

Be careful when changing the BIOS settings. The IPC system might not boot if false modifications were made. Refer to chapter 8.2 for the BIOS recovery option.



#### 9.1.2. Main menu

In order to modify BIOS settings <F2> has to be press while booting the IPC/ML71 system. The following main menu will appear:

				Phoen	ix Seco	ureCore	Tiano Se	etup	
Mai	n	Adva	unced	Sec	urity	Boot	Exi	t	
Sust	en Dat	te		[ <b>11</b> /01	/20101		1111	Item	Specific Help
Syst Syst > Syst > Boot > Erro	iem Dat iem Tin iem Ini : Feati ir Mand	te ne forma ures ager	tion	( <b>0</b> ):44	72010] :06]			View on date.	r set system
11									
F1 Esc	Help Exit	1↓ ↔	Select	Item	+/- Enter	Change Select	Values ▶ Suh-M	F9 S enu F10 S	etup Defaults ave and Exit

Fig. 25 BIOS setup main menu

The system time and date can be modified in this menu. Also some system information is provided in the submenu *System Information*.

Phoenix SecureCore Tiano Setup						
	System Information					
BIOS Version Build Time Processor Type Processor Speed System Memory Speed L2 Cache RAM Total Memory Memory Mode Memory Channel A Slot 0 Memory Channel A Slot 1 Memory Channel B Slot 1	QB_2.1.0.409 IA32 12/06/2012 Intel(R) Atom(TM) CPU E680 @ 1.60GHz 1.60 GHz 800 MHz 512 KB 2048 MB Memory MODE_DUAL_INTERLEAVE 2048 MB (DDRIII800)					
F1 Help 1↓ Select Ite Esc Exit ↔ Select Men	m +/- Change Values F9 Setup Defaults µ Enter Select ▶ Sub-Menu F10 Save and Exit					

Fig. 26 System information



#### 9.1.3. Advanced



Fig. 27 Advanced menu

In the sub menu *Baseboard Peripherals* and then *SIO* different resources can be assigned to the UARTs.



Fig. 28 Baseboard Peripherals sub menu



Phoenix SecureCore Tiano Setup Advanced						
LPC Configura	tion	Item Specific Help				
Onboard Floppy Controller	[Disabled]	This option controls				
Onboard Keyboard Controller	[Enabled]	Address. When				
Onboard Parallel Port	[Disabled]	address 0x3F8h and IRO 3, 4, 5, 6, 7, 9,				
Onboard UART1	[Enabled]	10, 11, 12.				
HART TRO						
RS-485 Auto Dir	[Disabled]					
Onboard UART2	[Enabled]	and the second				
UARI Base Address	L2F8hJ	and the second second				
DE AGE Quite Din	[J]					
N3-403 NULU D11.						
F1 Help 14 Select Item ↔ Esc Exit ↔ Select Menu F	/- Change Values nter Select ► Sub-Menu	F9 Setup Defaults F10 Save and Exit				

Fig. 29 SIO sub menu

Ph Advanced	oenix SecureCore Tiano Se	etup
LPC Conf	iguration	Item Specific Help
RS-485 Auto Dir Onboard UART3 UART Base Address UART IRQ RS-485 Auto Dir Onboard UART4 UART Base Address UART IRQ RS-485 Auto Dir Onboard UART5 Onboard UART6	Disabled] (Enabled) (3E8h) (5) (Disabled) (Enabled) (2E8h) (6) (Disabled) (Disabled) (Disabled)	This option controls the Onboard UART6 Address. When enabled. UART6 uses address 0x2A08h and IRQ 3, 4, 5, 6, 7, 9, 10, 11, 12.
F1 Help 14 Select It Esc Exit ↔ Select Me	em +/- Change Values nu Enter Select.▶ Sub-M	F9 Setup Defaults enu F10 Save and Exit

Fig. 30 UART configuration options



#### 9.1.4. Security

No modifications should be made here.



Fig. 31 Security menu

#### 9.1.5. Boot

In this menu the boot order can be changed.

Phoenix SecureCore Tiano Setup						
Main	Advanced	Secur i ty	Boot	Exit		
Boot F 1. 2.	Priority Order ATA HDD1: WDC ATA HDD0: ATA HDD0:	SSD-C0016S-7	150		Item Specific Help Keys used to view or	
3. 4. 5. 6. 7. 8.	ATAPI CD0: USB HDD: USB CD: USB FDD: SD Card0:				configure devices: T and 4 arrows Select a device. '+' and '-' move the device up or down. 'Shift + 1' enables or disables a	
9. 10. 11.	SD Card1: Internal Shel PCI LAN:	1			device. 'Del' deletes an umprotected device.	
F1 He	elp 14 Select	Item */-	Change Valu	les	F9 Setup Defaults F10 Same and Fait	

Fig. 32 Boot menu





#### 9.1.6. Exit

Different options can be selected to exit the BIOS setup.

М- 3		A1.		Phoen	ix Secu	ireCore	Tiand	o Setu	p		<u>.</u>
nai	I	Нача	inced	Sec	urity	Boot		Exit	_		
Exit Exit	t Savin t Disca	ng Ch urdir	nanges 19 Chano	ies					Ite	em Specific H	elp
Load	l Setur 1 Ontin	) Def	aults Defaul	lts					Equal	to F10, sa	ve 1
Disc	card Cl	nange	25						menus	, then exit	
Guv	2 Onun	100							drive reset	er. Finally to the system natically.	
											-
											-
F1 Esc	Help Exit	11 ++	Select	Item Menu	+/- Enter	Change Select	Valu ▶ Su	es h-Menu	F9 F10	Setup Defaul Save and Exi	ts t

Fig. 33 Exit menu

### 9.2. Application programming interface (API)

The RPC71 does not contain any special API besides the installed BIOS.



### 9.3. Operating systems

Syslogic offers an implementation for the following operating systems (OS):

Windows Embedded Standard 2009



Debian Linux Distribution *IPC/DEBIAN-60A* 

Microsoft Windows Embedded Standard 2009 *IPC/WINESTD09-71A* 

Windows Embedded Standard 7 Microsoft Windows Embedded 7 IPC/WINESTD7-71A

Others on request.

**Important note** When implementing a BSP for a new OS be sure to use the "Pentium Platform".



# **10Product revision history**

### 10.1. Hardware

This paragraph lists the different hardware revisions of the RPC71 delivered beginning with the first production lot. Note that prototyping boards are not included and must be returned to factory for upgrade or replacement. All information listed in this document relies on definitive state hardware. Therefore this information may be incompatible with the prototyping board hardware.

Board Identification (see product label)	Product Revision	Logic Design Revision ID	Remarks
RPC/SL71F16-1BCIVE	#1	n/a	First release, superseded
RPC/SL71F16-A101E	#1	0x06	New release with new baseboard
SDB/SL71F16-WI1	#1	n/a	First release
	#1.1	n/a	Termination removed from CAN interfaces
	#2.0	0x04	New baseboard (CFast support)
	#2.1	0x04	8GB CF included
	#2.2	0x04	Changed to CFast
	#3	tbd	New baseboard

Tab. 66 Hardware revision state



### 10.2. Firmware/BIOS

Board Identification (see product label)	<b>BIOS Version</b>	Remarks
RPC/SL71F16-1BCIVE		check CMOS setup information screen
RPC/SL71F16-A101E		check CMOS setup information screen
SDB/SL71F16-WI1		check CMOS setup information screen

Tab. 67 BIOS revision state

#### Important note

This document always covers the latest product revision listed in Tab 28. Please contact the manufacturers technical support for upgrade options.



# 11 Manufacturer information

### 11.1. Contact

Our distributors and system integrators will gladly give you any information about our products and their use. If you want to contact the manufacturer directly, please send a fax or email message containing a short description of your application and your request to the following address or use one of the information or technical support request forms on our internet homepage:

Syslogic Datentechnik AG Täfernstrasse 28 CH-5405 Baden-Dättwil / Switzerland

 Email:
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 www:
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 Phone
 +41 (0)56 200 90 40

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 +41 (0)56 200 90 50

Technical support: support@syslogic.com